Διπολικά Transistor

7/12/2020

Μάθημα 8ο

Transistor Specification Sheet
Τεχνικό Δελτίο

2N4123, 2N4124

General Purpose Transistors

NPN Silicon

Features

- Pb–Free Packages are Available*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage 2N4123 2N4124	V_{CEO}	 30 25	Vdc
Collector–Base Voltage 2N4123 2N4124	V_{CBO}	 40 30	Vdc
Emitter–Base Voltage	V_{EBO}	5.0	Vdc
Collector Current – Continuous	I_C	200	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12	W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	83.3	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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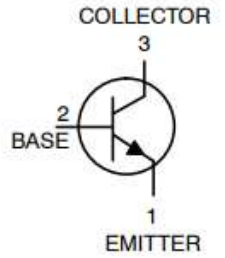
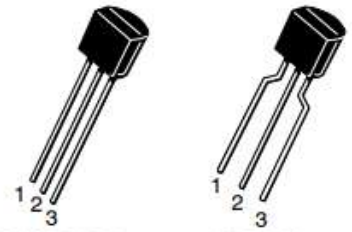


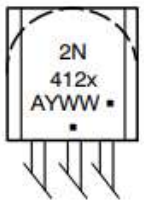
TO–92
CASE 29
STYLE 1



STRAIGHT LEAD
BULK PACK

BENT LEAD
TAPE & REEL
AMMO PACK

MARKING DIAGRAM



Transistor Specification Sheet

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (Note 1) (I_C = 1.0 mAdc, I_E = 0)	2N4123 2N4124	$V_{(BR)CEO}$	 30 25	 – –	Vdc
Collector–Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	2N4123 2N4124	$V_{(BR)CBO}$	 40 30	 – –	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)		$V_{(BR)EBO}$	5.0	–	Vdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0)		I_{CBO}	–	50	nAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)		I_{EBO}	–	50	nAdc
ON CHARACTERISTICS					
DC Current Gain (Note 1) (I_C = 2.0 mAdc, V_{CE} = 1.0 Vdc) (I_C = 50 mAdc, V_{CE} = 1.0 Vdc)	2N4123 2N4124 2N4123 2N4124	h_{FE}	50 120 25 60	150 360 – –	–
Collector–Emitter Saturation Voltage (Note 1) (I_C = 50 mAdc, I_B = 5.0 mAdc)		$V_{CE(sat)}$	–	0.3	Vdc
Base–Emitter Saturation Voltage (Note 1) (I_C = 50 mAdc, I_B = 5.0 mAdc)		$V_{BE(sat)}$	–	0.95	Vdc
SMALL–SIGNAL CHARACTERISTICS					
Current–Gain – Bandwidth Product (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	2N4123 2N4124	f_T	250 300	– –	MHz
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)		C_{ibo}	–	8.0	pF
Collector–Base Capacitance (I_E = 0, V_{CB} = 5.0 V, f = 1.0 MHz)		C_{cb}	–	4.0	pF
Small–Signal Current Gain (I_C = 2.0 mAdc, V_{CE} = 10 Vdc, R_S = 10 k Ω, f = 1.0 kHz)	2N4123 2N4124	h_{fe}	50 120	200 480	–
Current Gain – High Frequency (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz) (I_C = 2.0 mAdc, V_{CE} = 10 V, f = 1.0 kHz) (I_C = 2.0 mAdc, V_{CE} = 10 V, f = 1.0 kHz)	2N4123 2N4124 2N4123 2N4124	$\lvert h_{fe} \rvert$	2.5 3.0 50 120	– – 200 480	–
Noise Figure (I_C = 100 μAdc, V_{CE} = 5.0 Vdc, R_S = 1.0 k Ω, f = 1.0 kHz)	2N4123 2N4124	NF	– –	6.0 5.0	dB

1. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

Transistor Specification Sheet

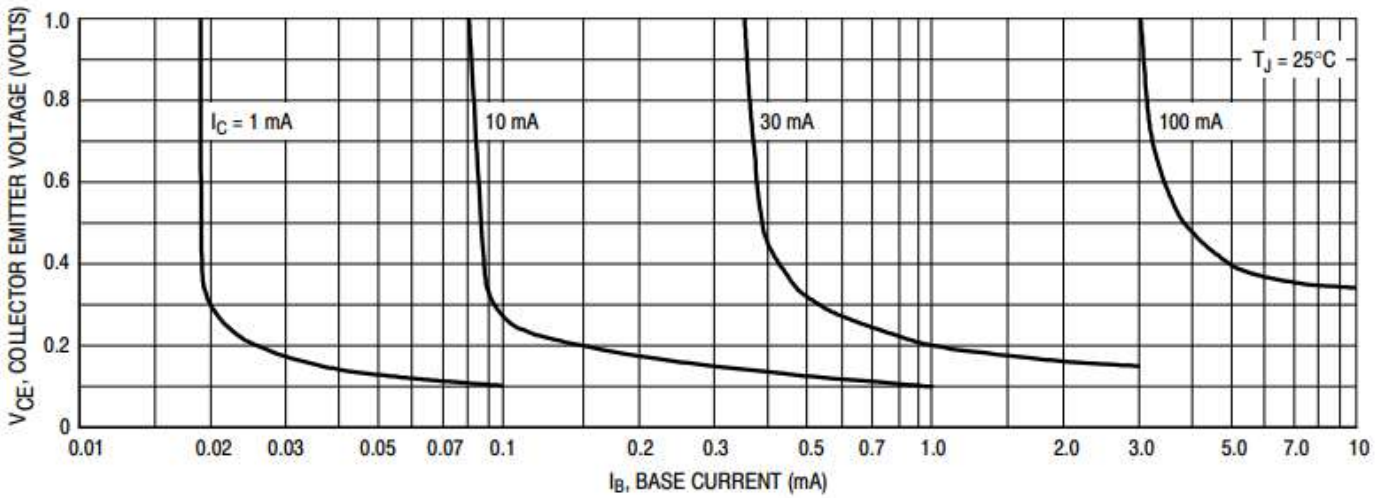


Figure 10. Collector Saturation Region

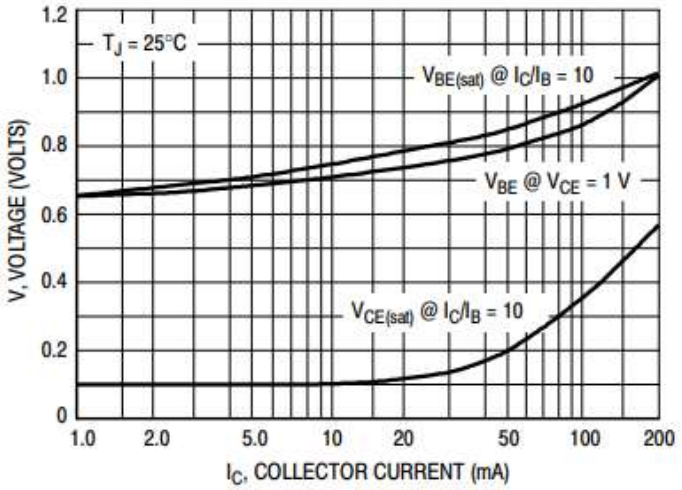


Figure 11. "On" Voltages

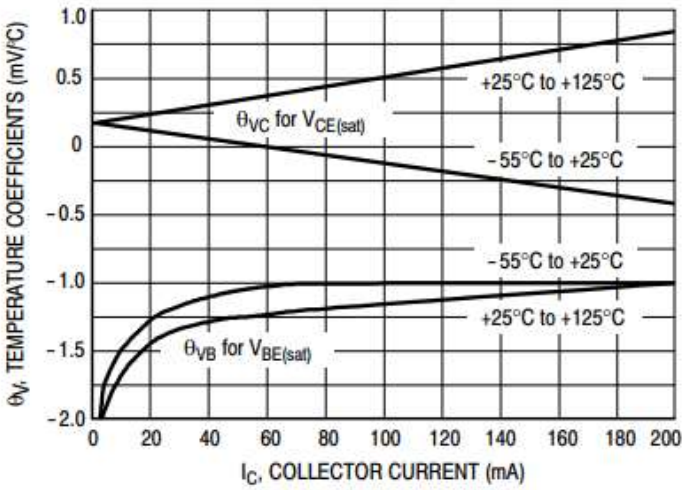
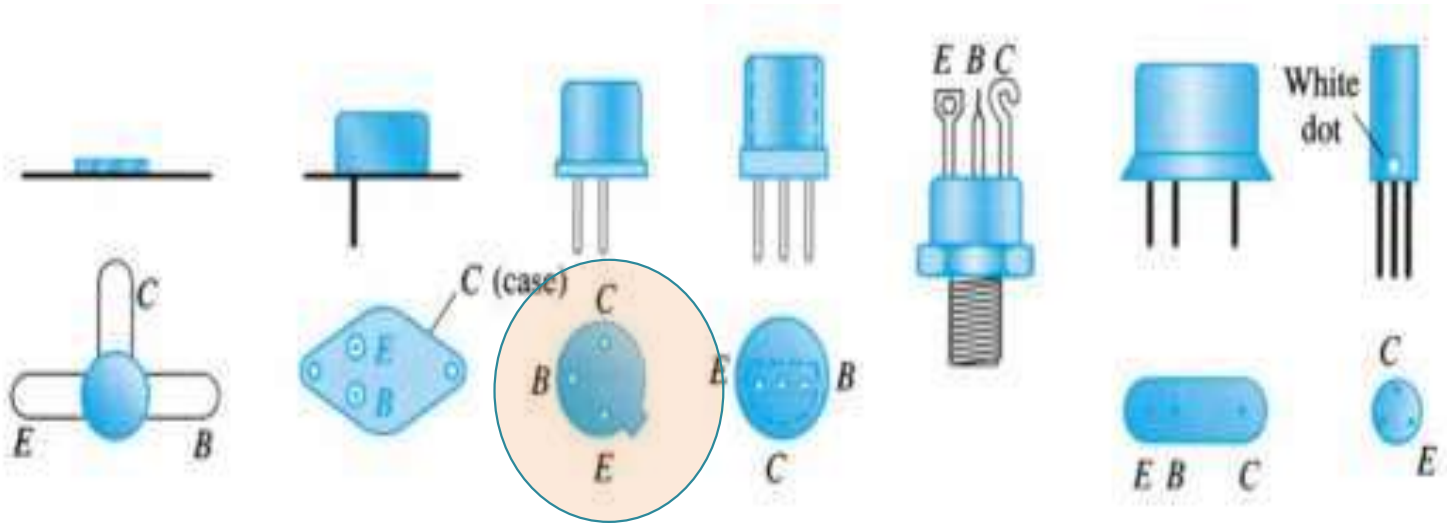


Figure 12. Temperature Coefficients

Transistor Terminal Identification

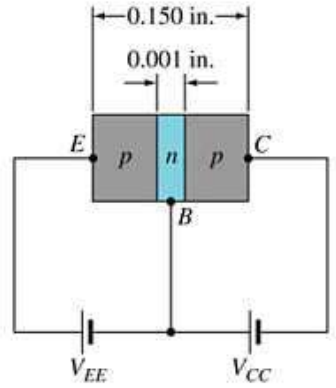


Transistor Construction

There are two types of transistors:

- *pnp*
- *npn*

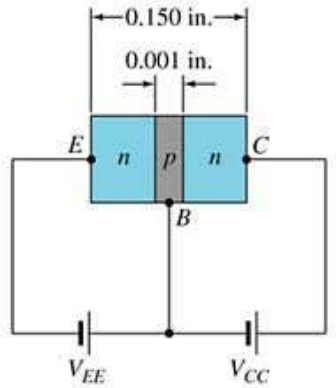
pnp

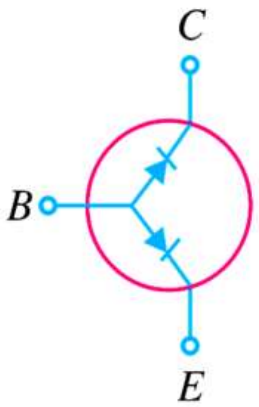


The terminals are labeled:

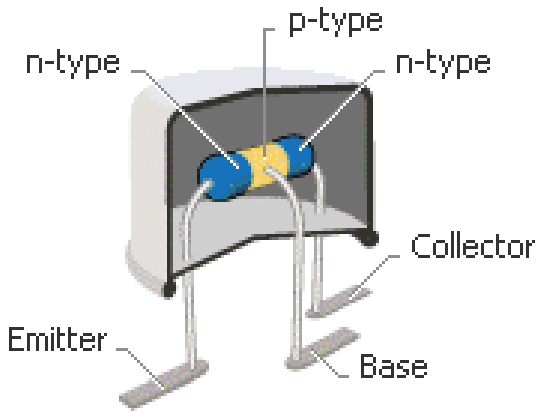
- E - Emitter
- B - Base
- C - Collector

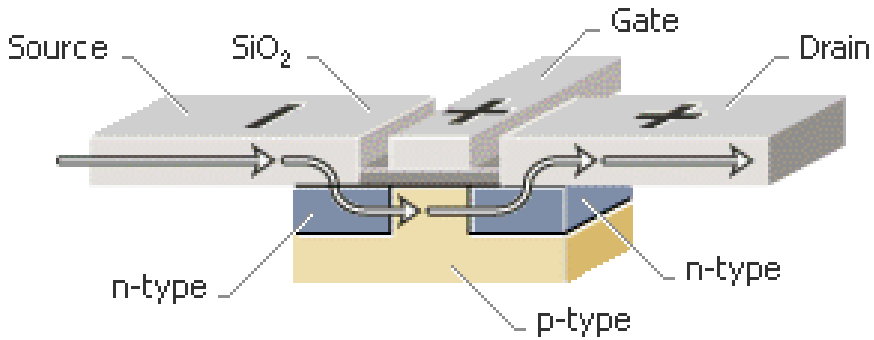
npn

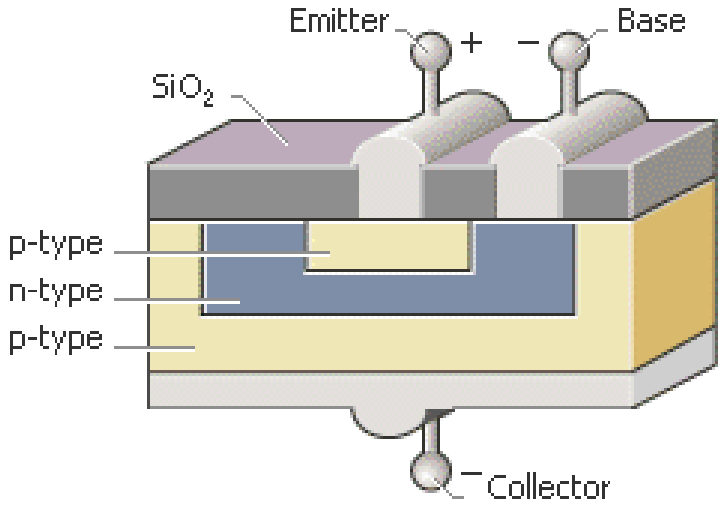


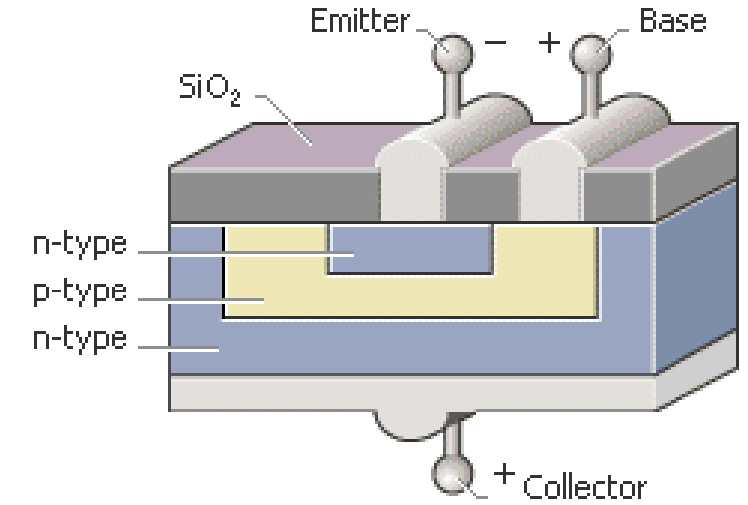


Δομή


p-type
n-type
n-type
Collector
Emitter
Base


Source
SiO_2
Gate
Drain
n-type
n-type
p-type

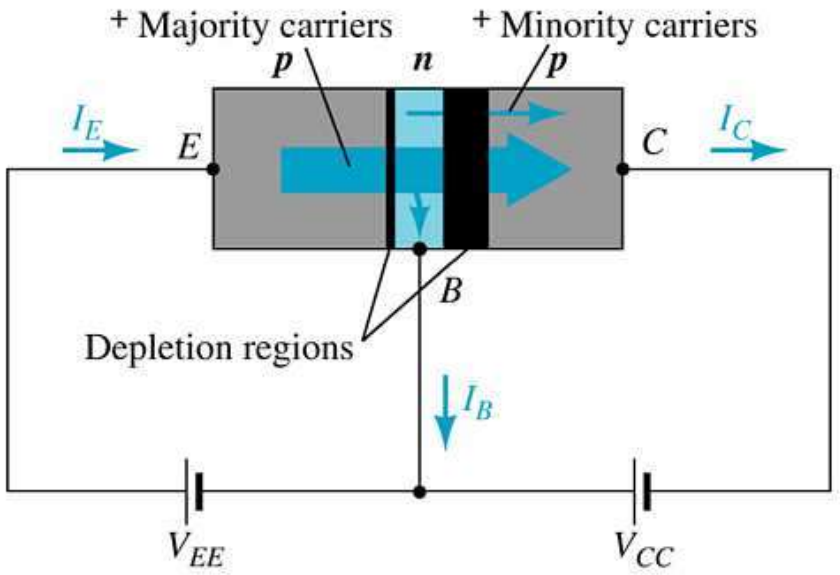

Emitter
+
−
Base
SiO_2
p-type
n-type
p-type
−
Collector

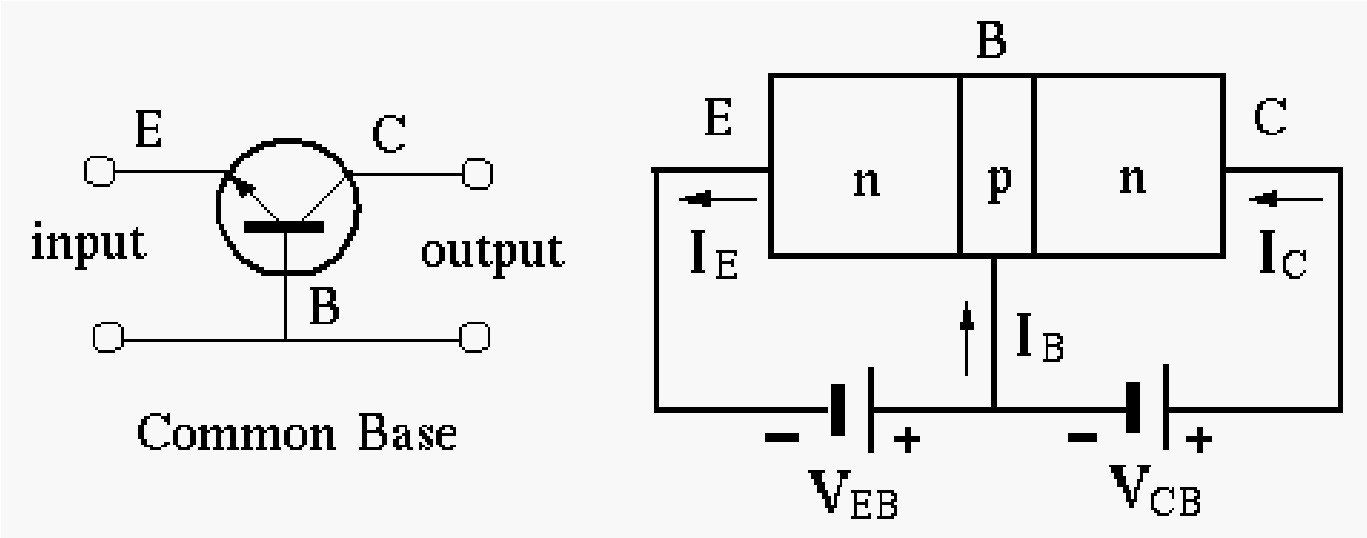

Emitter
−
+
Base
SiO_2
n-type
p-type
n-type
+
Collector

Λειτουργία του (BJT)ransistor Operation

With the external sources, V_{EE} and V_{CC}, connected as shown:

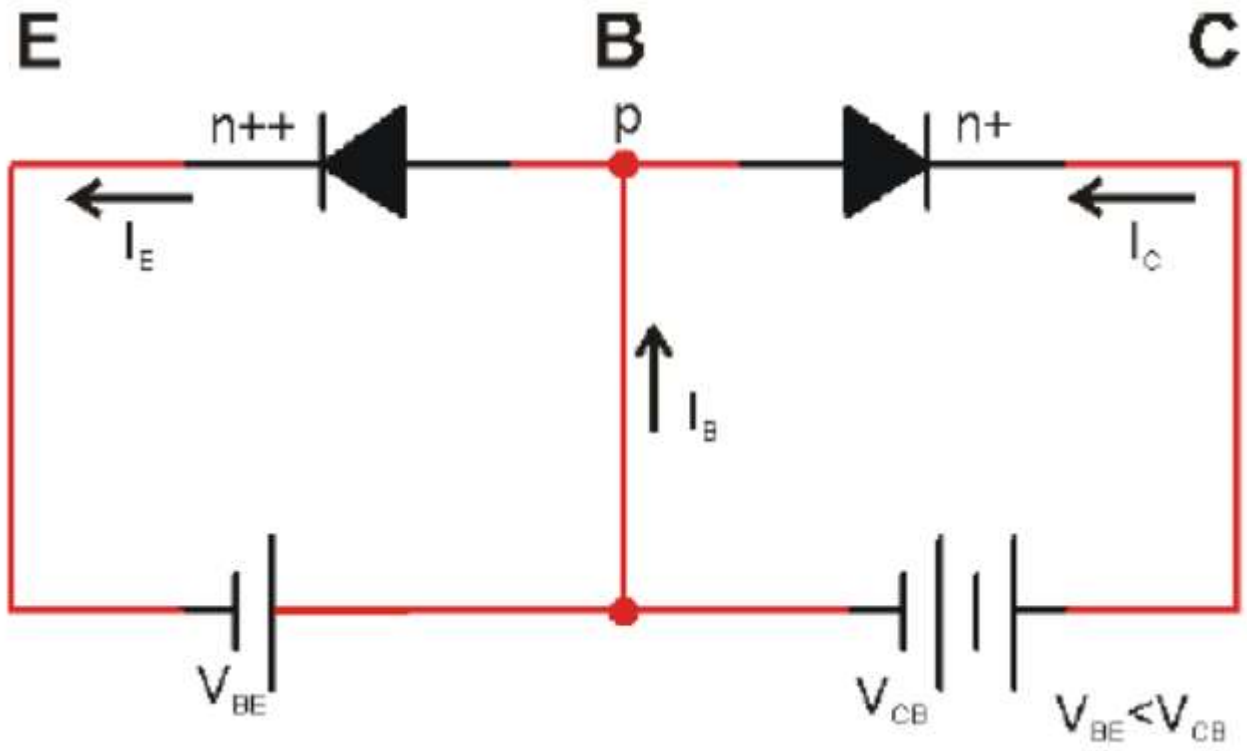
- The emitter-base junction is forward biased
- The base-collector junction is reverse biased

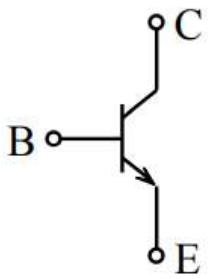




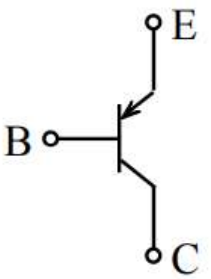
$$I_E = I_B + I_C$$

Φυσική Λειτουργία



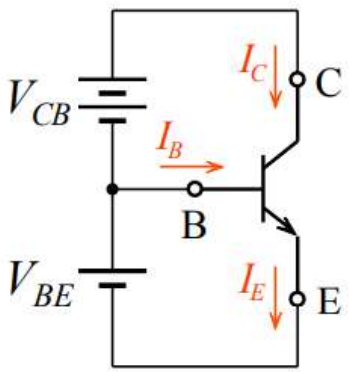


Τύπος npn



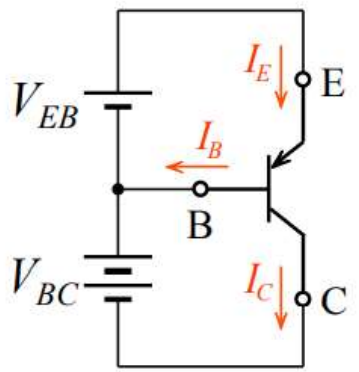
Τύπος pnp

Κυκλωματικοί συμβολισμοί των διπολικών τρανζίστορ



$$V_{CE} = V_{CB} + V_{BE}$$

$$I_E = I_C + I_B$$



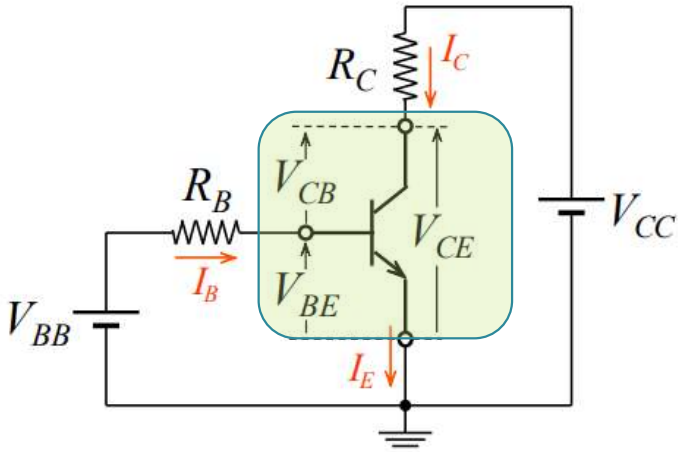
$$V_{EC} = V_{BC} + V_{EB}$$

$$I_E = I_C + I_B$$

Παράμετροι του

$I_C = \beta I_B + (\beta+1) I_{CBO}$

$I_{CBO} = 0$



$$I_C = I_S \cdot e^{\frac{V_{BE}}{V_T}}$$

$$I_B = \frac{I_C}{\beta} = \frac{I_S}{\beta} \cdot e^{\frac{V_{BE}}{V_T}}$$

$$I_E = \frac{\beta+1}{\beta} \cdot I_S \cdot e^{\frac{V_{BE}}{V_T}} = \frac{1}{a} \cdot I_S \cdot e^{\frac{V_{BE}}{V_T}}$$

$$I_C = \beta \cdot I_B$$

$$V_{BE} \approx 0{,}7\,\mathrm{V}$$

$$I_E = \frac{I_B}{\alpha}$$

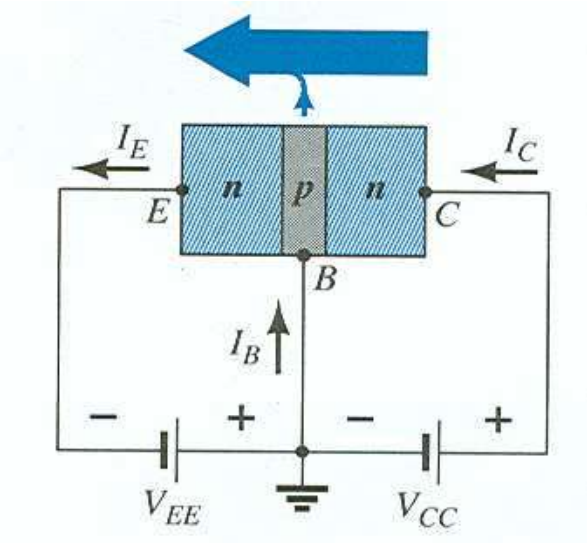
$$V_{BB} = I_B \cdot R_B + V_{BE} \Longrightarrow I_B = \frac{V_{BB} - V_{BE}}{R_B}$$

$$\beta = \frac{\alpha}{1-\alpha} \qquad \alpha = \frac{\beta}{\beta+1}$$

$$V_{CE} = V_{CC} - I_C \cdot R_C$$

$$V_{CB} = V_{CE} - V_{BE}$$

Currents in a Transistor



Emitter current is the sum of the collector and base currents:

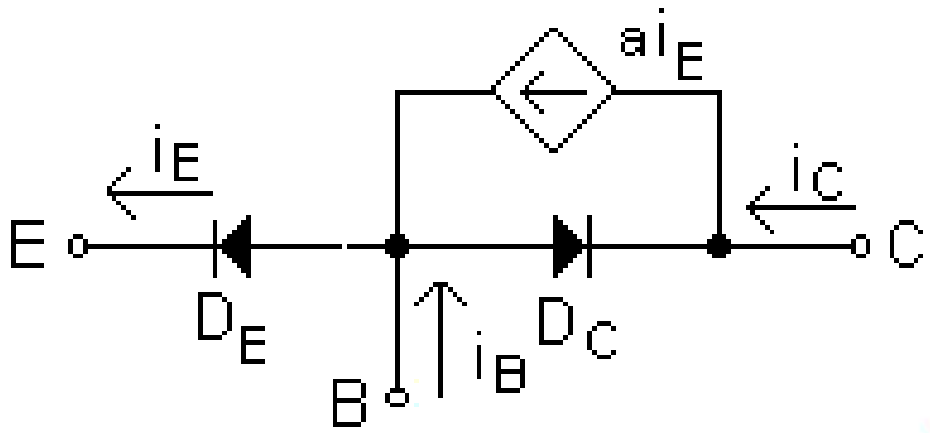
$$I_E = I_C + I_B$$

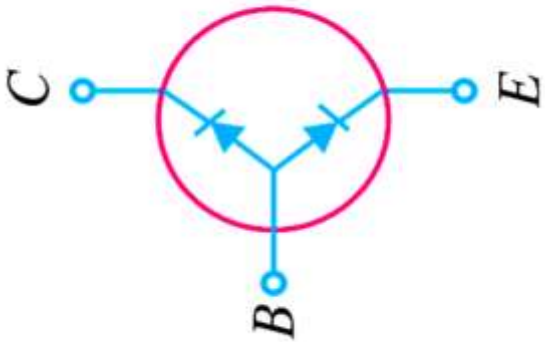
The collector current is comprised of two currents:

$$I_C = I_{C_{majority}} + I_{CO_{minority}}$$

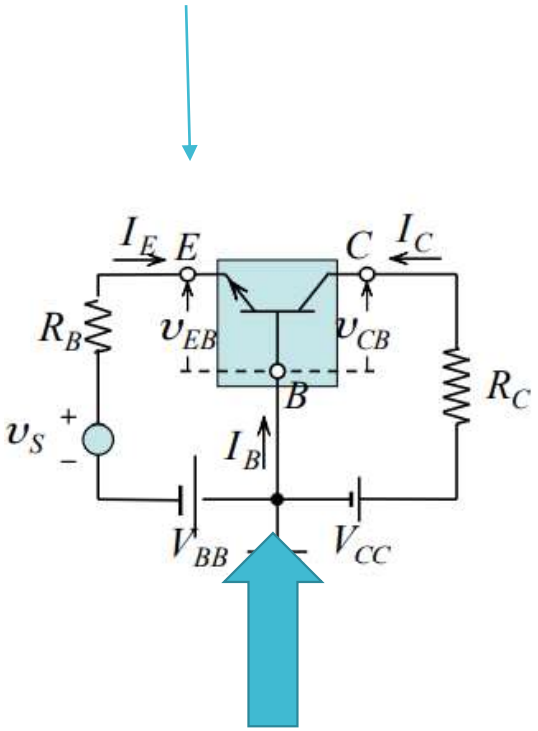
Τρόποι συνδεσμολογίας

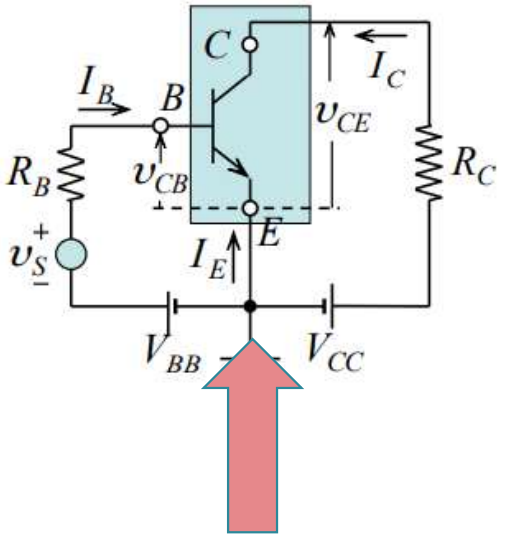
- Ένα NPN τρανζίστορ είναι πολωμένο έτσι ώστε ο συλλέκτης να είναι σε ένα θετικότερο δυναμικό από ότι η βάση και επομένως η δίοδος DC είναι ανάστροφα πολωμένη και μπορεί να αγνοηθεί.

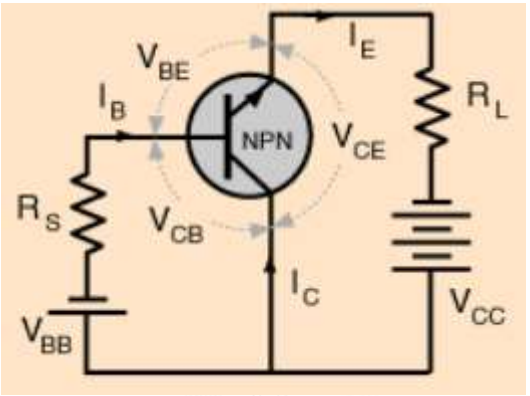




КВ, КЕ, КΣ


I_E
E
C
I_C
R_B
v_{EB}
v_{CB}
B
R_C
v_S
I_B
V_{BB}
V_{CC}

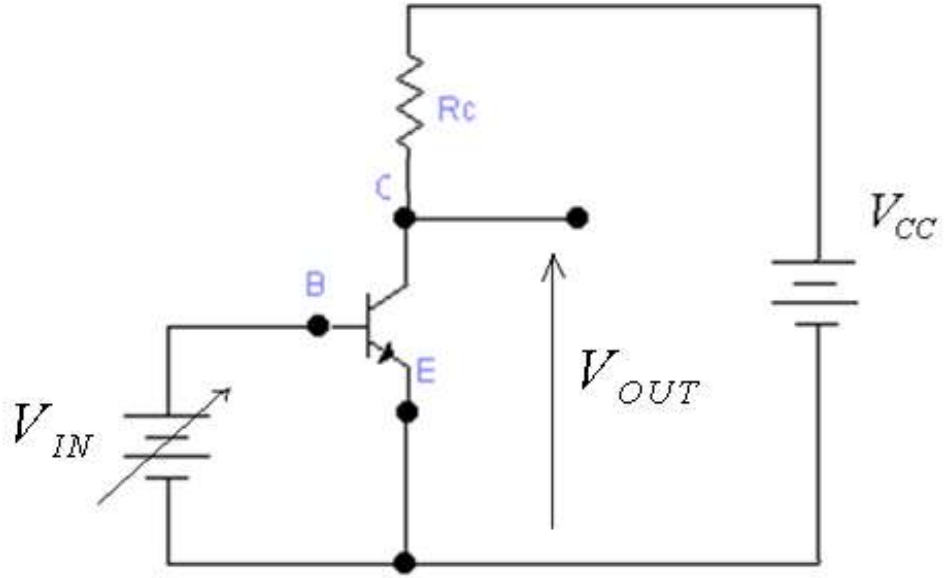

I_B
B
C
I_C
v_{CE}
R_B
v_{CB}
R_C
v_S
I_E
E
V_{BB}
V_{CC}


V_{BE}
I_E
I_B
NPN
V_{CE}
R_L
R_S
V_{CB}
I_C
V_{BB}
V_{CC}

Χρήσεις

- Διακόπτης
- Ενισχυτής

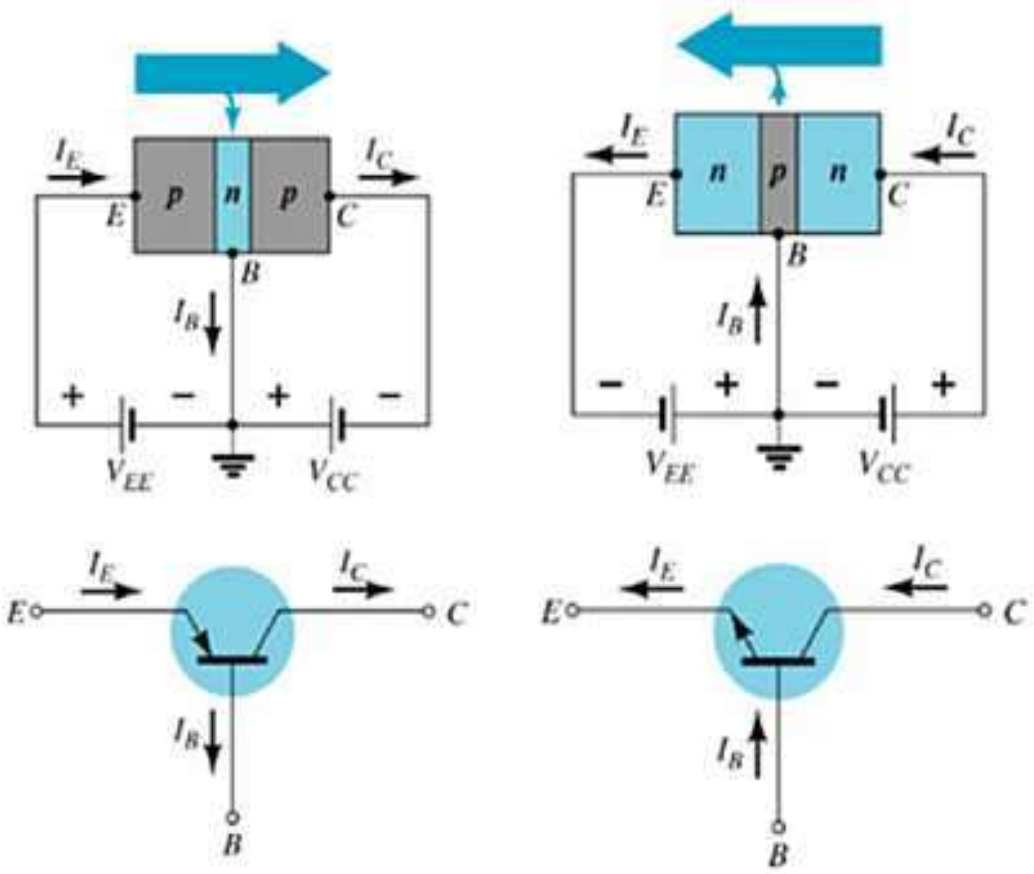
Ενισχυτής κοινού εκπομπού (ΚΕ) (Θεμελιώδες κύκλωμα)



$$V_{OUT} = V_{CC} - R_C I_C = V_{CC} - R_C I_S e^{\frac{V_{IN}}{V_T}}$$

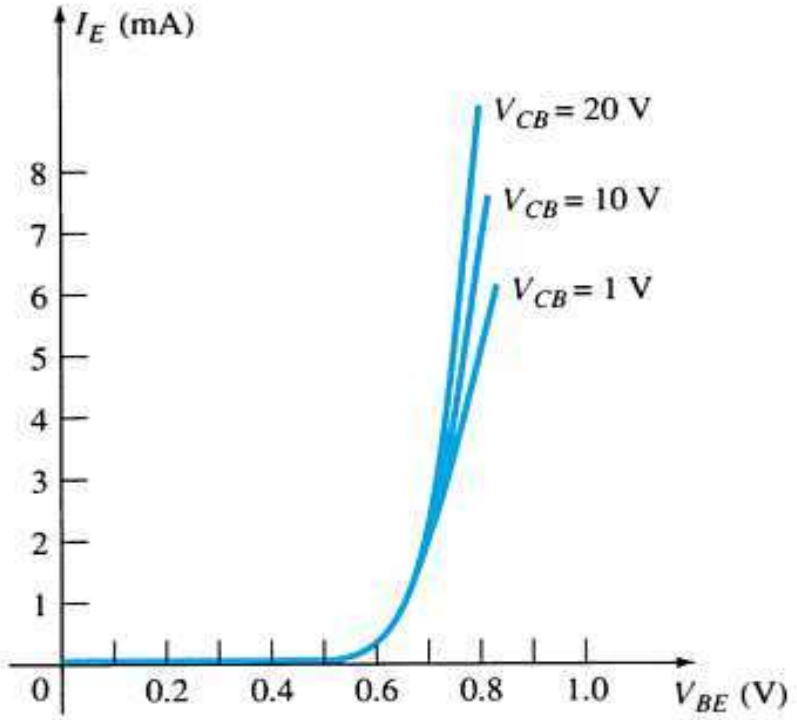
$$V_{CC} = 20V, R_C = 10K\Omega, I_S = 10^{-14} A, V_T = 25mV$$

Common-Base Configuration



The base is common to both input (emitter–base) and output (collector–base) of the transistor.

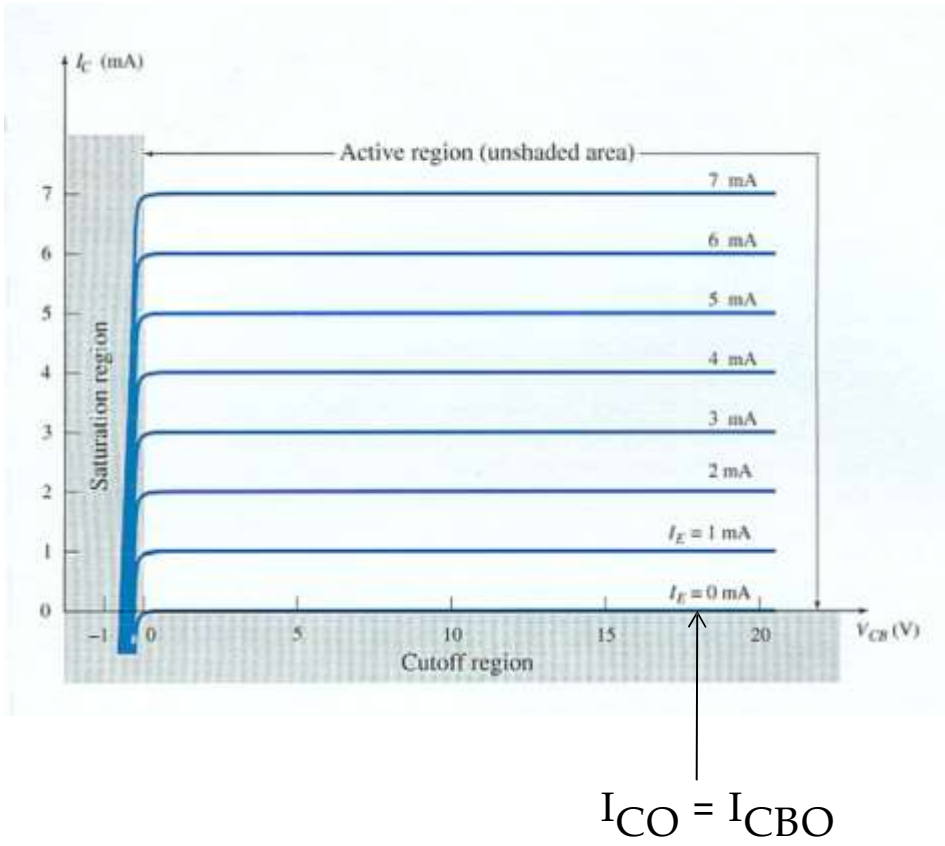
Common-Base Amplifier (Εισοδος)



Input Characteristics

This curve shows the relationship between of input current (I_E) to input voltage (V_{BE}) for three output voltage (V_{CB}) levels.

Common-Base Amplifier (Έξοδος)



Output Characteristics

This graph demonstrates the output current (I_C) to an output voltage (V_{CB}) for various levels of input current (I_E).

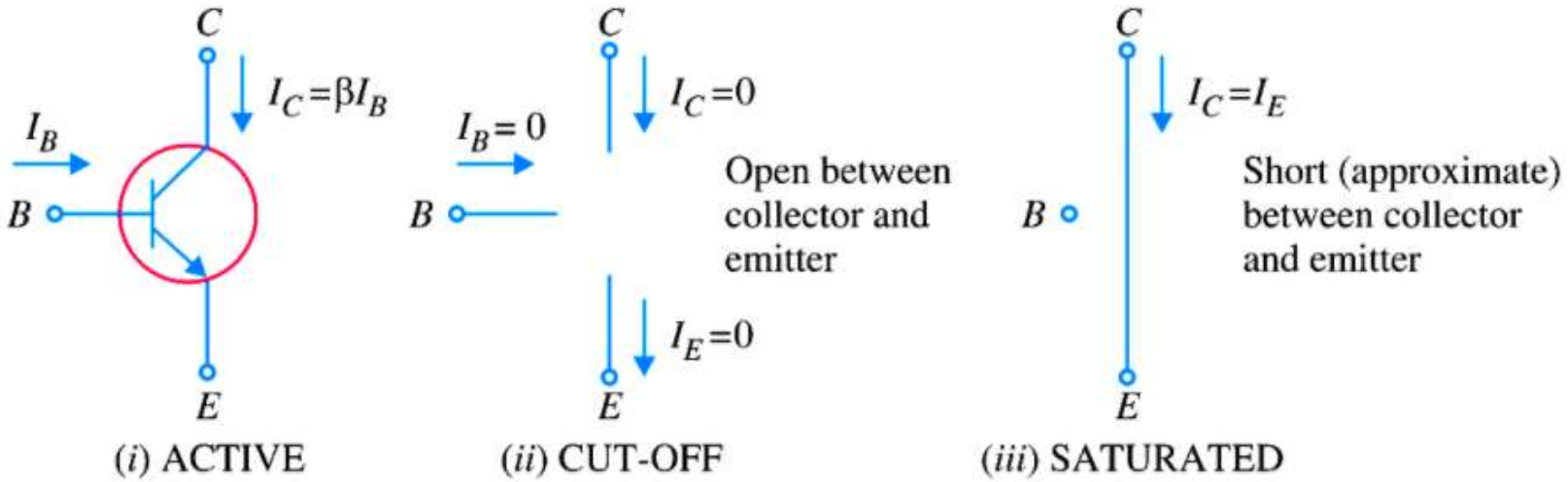
Operating Regions
Τρόποι Λειτουργίας

Τρόπος λειτουργίας	Πόλωση εκπομπού – βάσης	Πόλωση συλλέκτη – βάσης
Αποκοπή	Ανάστροφη	Ανάστροφη
Ενεργός	Ορθή	Ανάστροφη
Κόρος	Ορθή	Ορθή
Μη ενεργός	Ανάστροφη	Ορθή

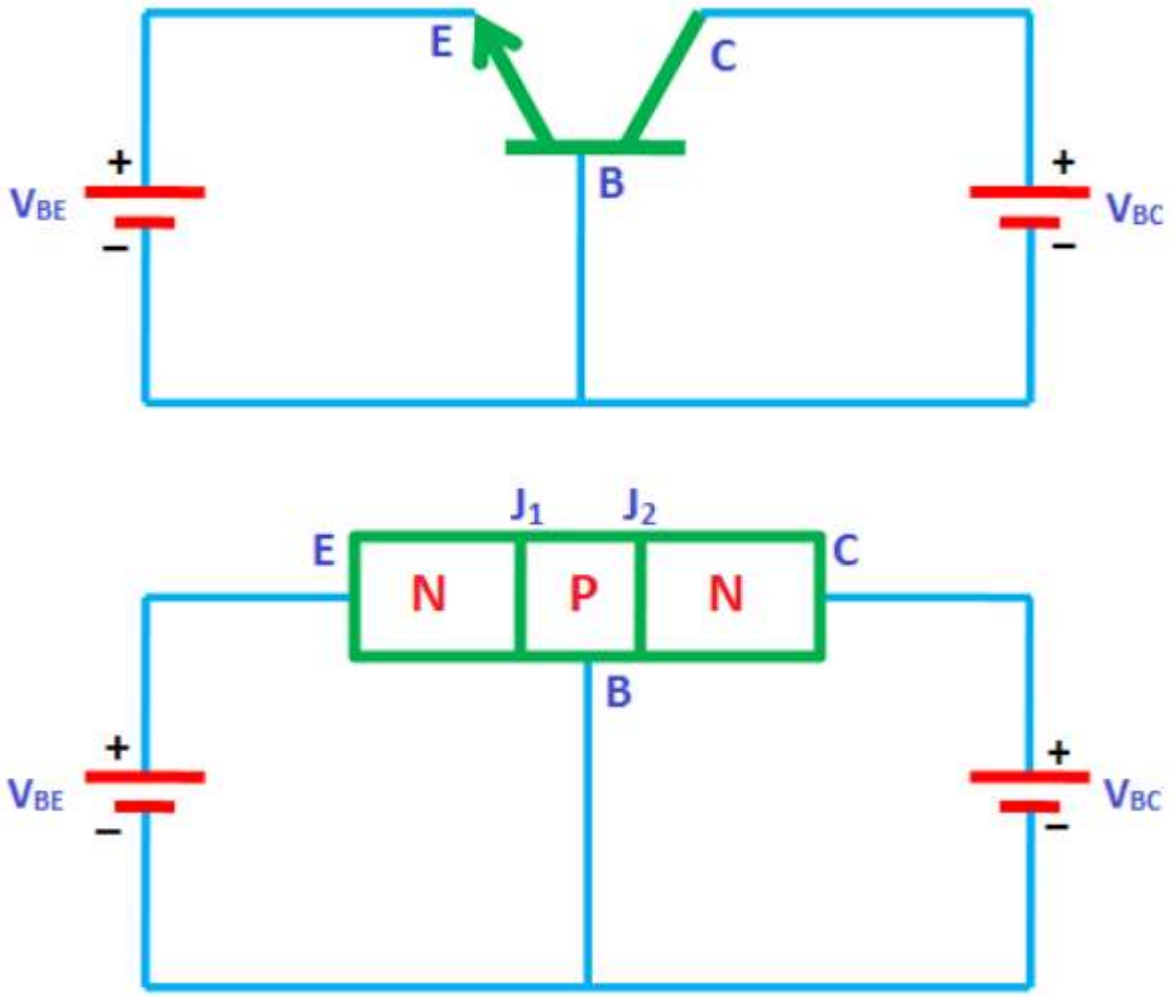
- Active – Operating range of the amplifier.
- Cutoff – The amplifier is basically off. There is voltage, but little current.
- Saturation – The amplifier is full on. There is current, but little voltage.

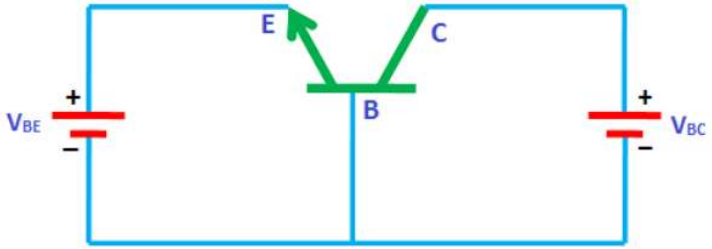
Regions	Base-Emitter	Collector-Base
Active	Forward-biased	Reverse-biased
Cutoff	Reverse-biased	Reverse-biased
Saturation	Forward-biased	Forward-biased

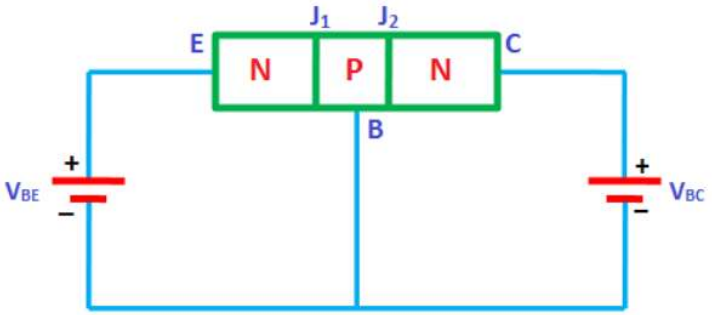
Λειτουργία


C
$I_C=\beta I_B$
I_B
B
E
(i) ACTIVE
$I_B=0$
C
$I_C=0$
B
Open between collector and emitter
$I_E=0$
E
(ii) CUT-OFF
C
$I_C=I_E$
B
Short (approximate) between collector and emitter
E
(iii) SATURATED

Αποκοπή







Αποκοπή

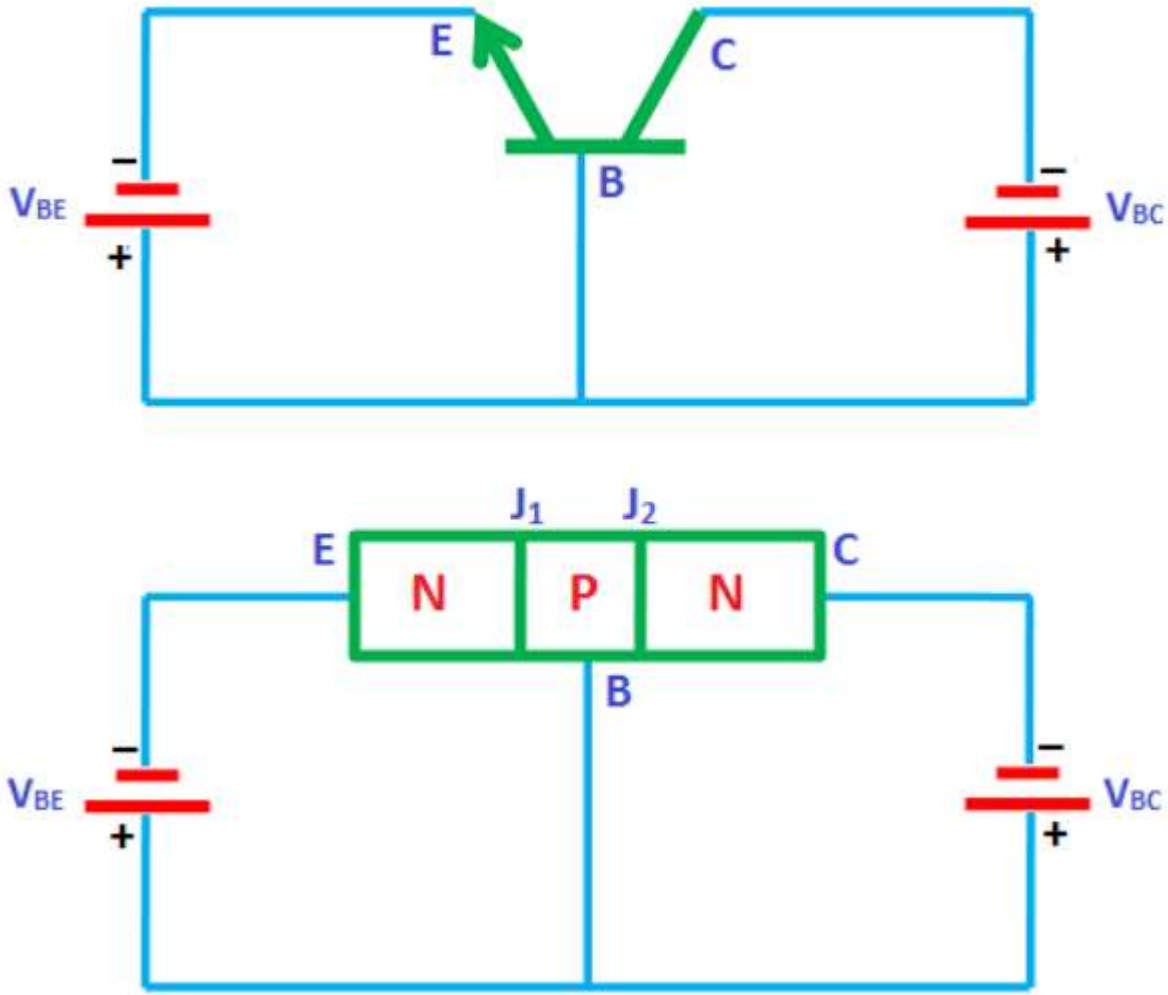
Επιτυγχάνεται εάν πολώσουμε

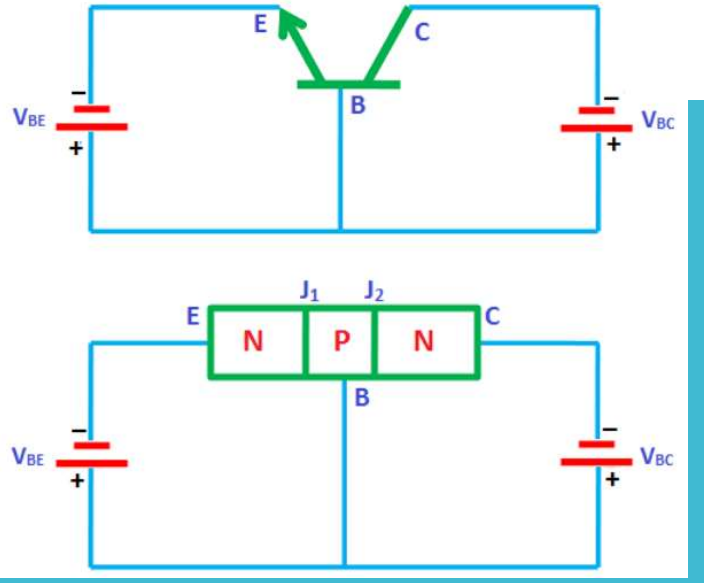
ανάστροφα εκπομπό - βάση και

ανάστροφα βάση - συλλέκτη.

Τότε και οι δύο περιοχές απογύμνωσης διευρύνονται με αποτέλεσμα να μην έχουμε διέλευση ρεύματος προς καμία κατεύθυνση παρά μόνο τα πολύ μικρά ανάστροφα ρεύματα εκπομπού - βάσης και βάσης - συλλέκτη.

Κόρος





Κόρος

Επιτυγχάνεται εάν πολώσουμε

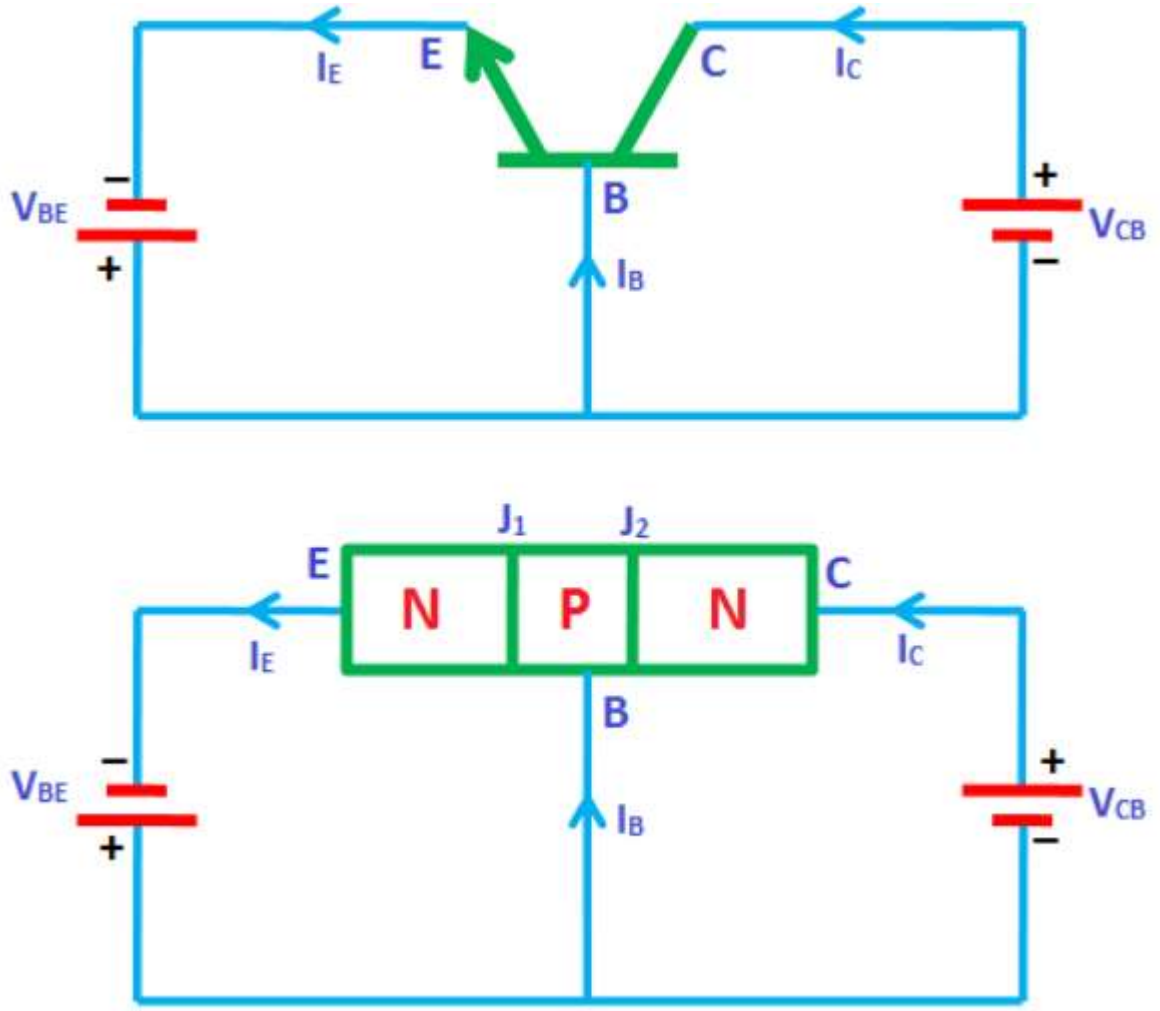
ορθά εκπομπό - βάση και

ορθά βάση - συλλέκτη

Τότε και οι δύο περιοχές απογύμνωσης συρρικνώνονται με αποτέλεσμα να έχουμε κίνηση οπών προς τη βάση **και από τον εκπομπό και από το συλλέκτη** με αποτέλεσμα να εμποδίζεται η διέλευση οπών από τον εκπομπό προς το συλλέκτη.

Έτσι ο φραγμός δυναμικού καταργείται τελείως και το τρανζίστορ συμπεριφέρεται σαν ένας κοινός αγωγός και θα πρέπει τα ρεύματα συλλέκτη και εκπομπού να περιορίζονται με εξωτερικές αντιστάσεις για να μην καταστραφεί το τρανζίστορ.

Ορθή λειτουργία Ενεργός περιοχή



Approximations
Παραδοχές

Emitter and collector currents:

$$I_E \cong I_C$$

Base-emitter voltage:

$$V_{BE} = 0.7\ \text{V (for Silicon)}$$

Alpha του BJT (α)

Alpha (α) is the ratio of I_C to I_E :

$$\alpha_{dc} = \frac{I_C}{I_E}$$

Ideally: α = 1
In reality: α is between 0.9 and 0.998

$$I_C = \alpha I_E + I_{CBO}$$

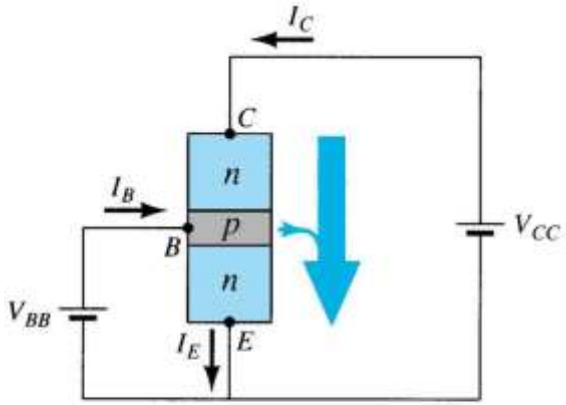
Alpha (α) in the AC mode:

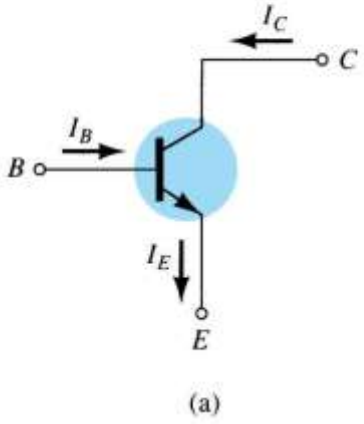
$$\alpha_{ac} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}} = \text{constant}$$

Common–Emitter Configuration KE

The emitter is common to both input (base-emitter) and output (collector- emitter).

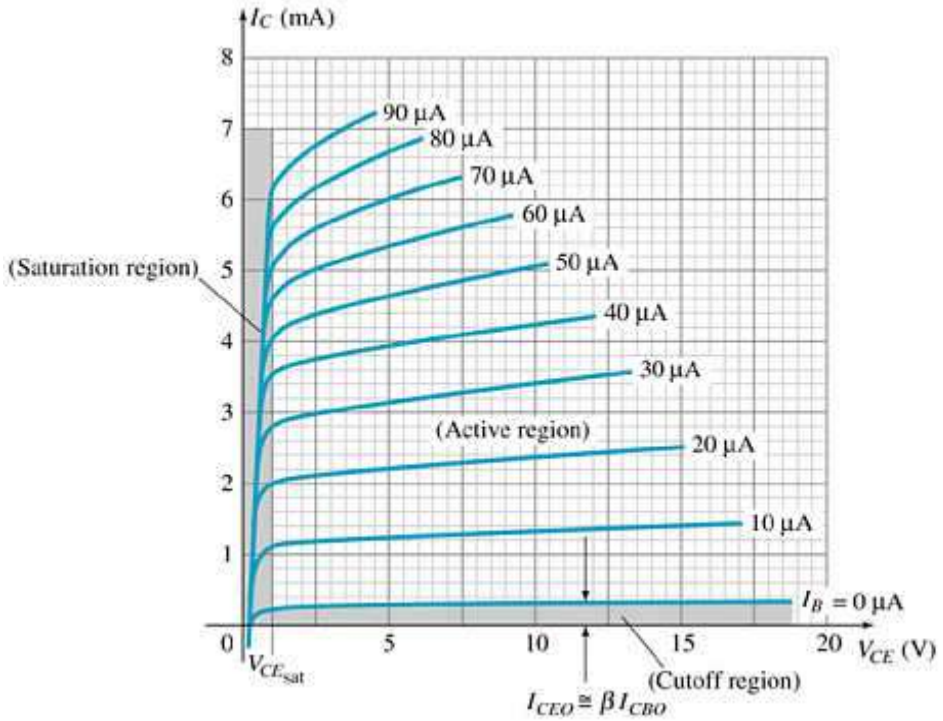
The input is on the base and the output is on the collector.



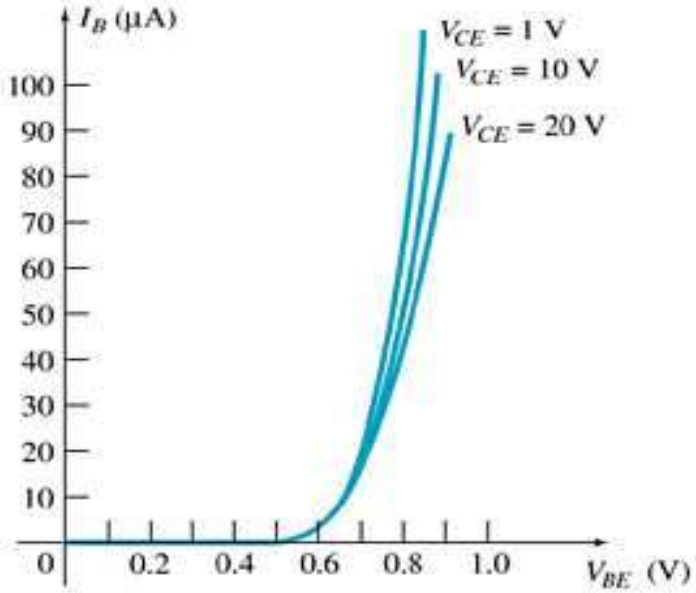


(a)

Χαρακτηριστικές Common-Emitter Characteristics

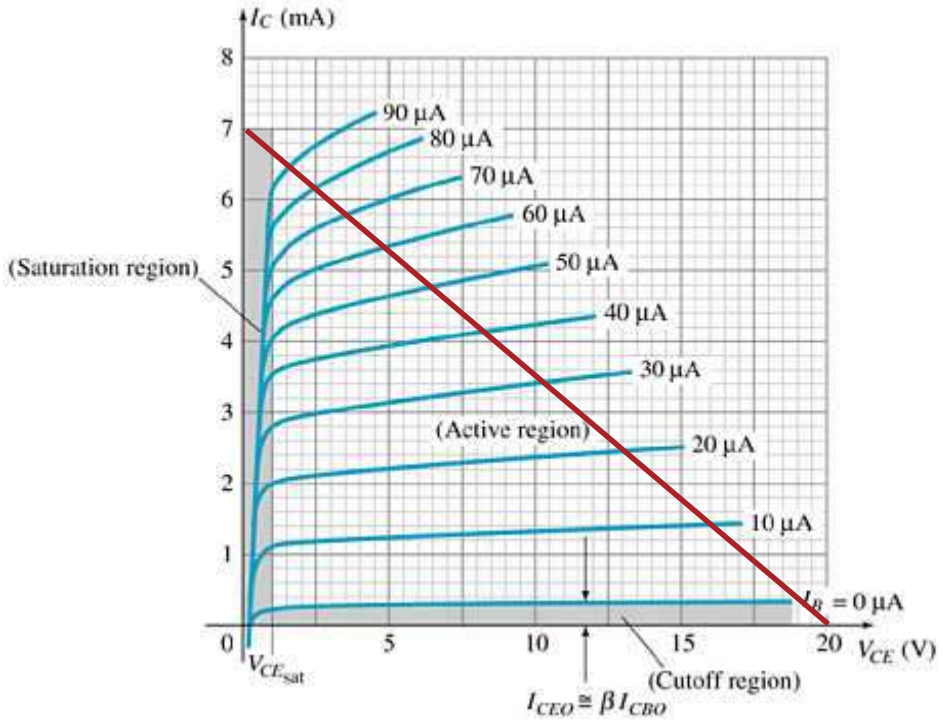


Collector Characteristics

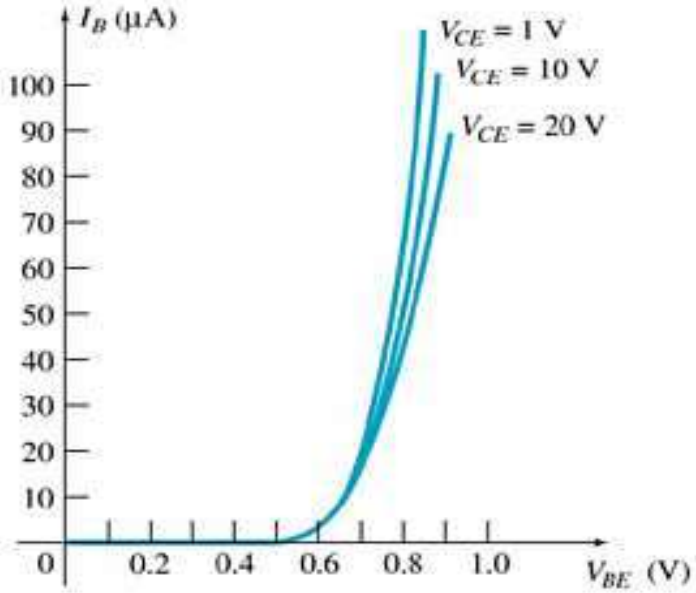


Base Characteristics

Χαρακτηριστικές Common-Emitter Characteristics



Collector Characteristics



Base Characteristics

Common-Emitter Amplifier Currents

Ideal Currents

$I_E = I_C + I_B$ $\qquad$ $I_C = \alpha I_E$

Actual Currents

$I_C = \alpha I_E + I_{CBO}$ $\qquad$ where I_{CBO} = minority collector current

I_{CBO} is usually so small that it can be ignored, except in high power transistors and in high temperature environments.

When $I_B = 0$ μA the transistor is in cutoff, but there is some minority current flowing called I_{CEO}.

$$I_{CEO} = \frac{I_{CBO}}{1-\alpha}\Big|_{I_B=0\,\mu A}$$

Beta του BJT (β)

β represents the amplification factor of a transistor. (β is sometimes referred to as h_{fe}, a term used in transistor modeling calculations)

In DC mode:

$$\beta_{dc} = \frac{I_C}{I_B}$$

In AC mode:

$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B}\Big|_{V_{CE}=constant}$$

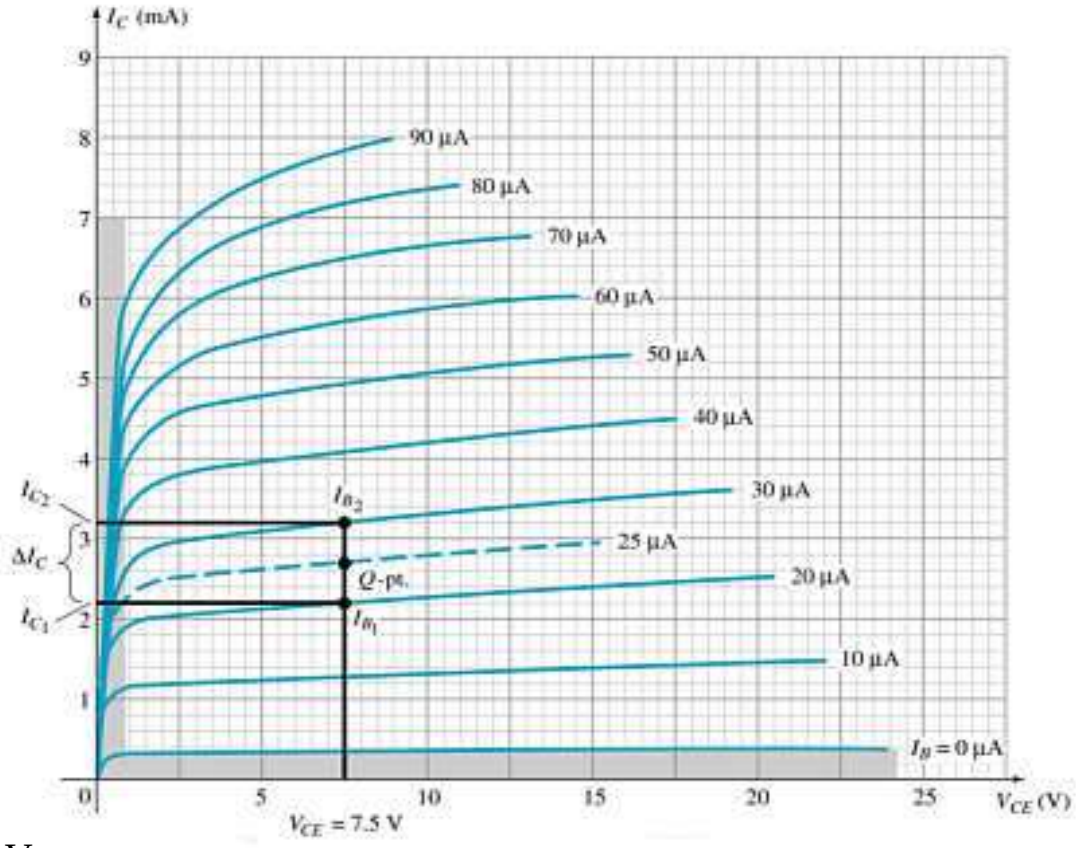
Beta (β)

Υπολογίζω το β από το γράφημα

$$\beta_{AC} = \frac{(3.2\text{mA} - 2.2\text{mA})}{(30\mu\text{A} - 20\mu\text{A})}$$

$$= \frac{1\,\text{mA}}{10\,\mu\text{A}}\Bigg|_{V_{CE}=7.5\text{ V}}$$

$$= 100$$



$$\beta_{DC} = \frac{2.7\text{ mA}}{25\ \mu\text{A}}\Bigg|_{V_{CE}=7.5\text{ V}}$$

$$= 108$$

Both β values are usually reasonably close and are often used interchangeably

Beta του BJT (β)

Relationship between amplification factors β and α

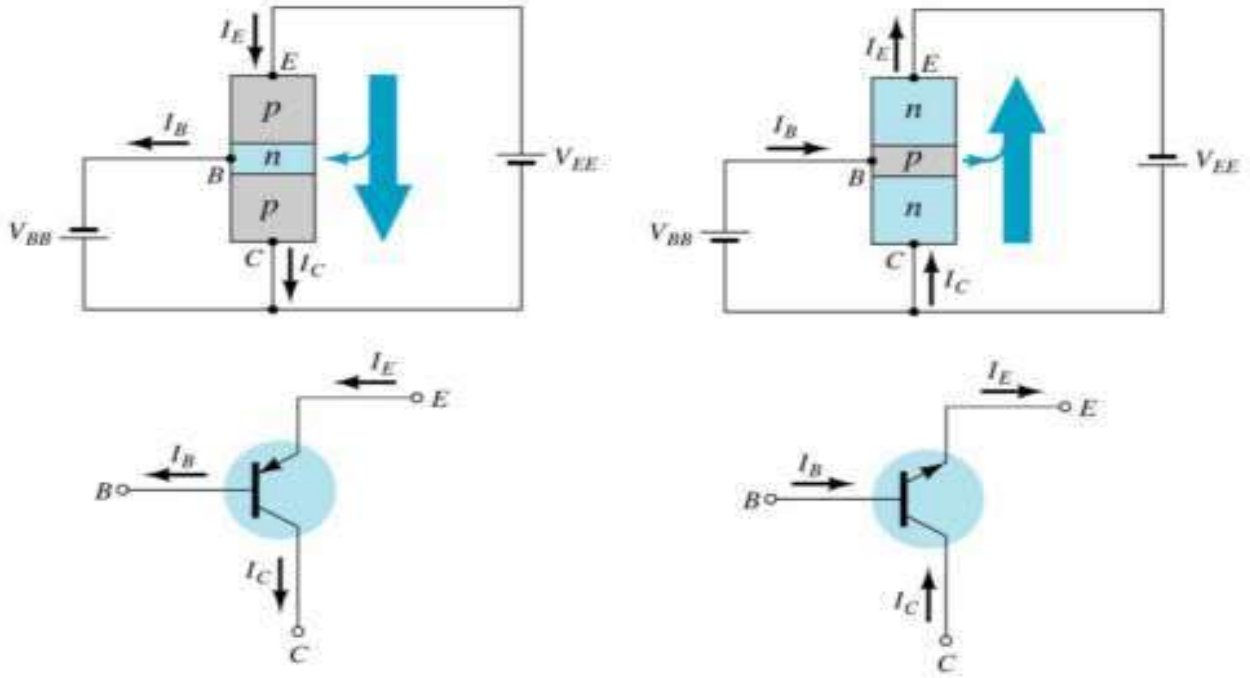
$$\alpha = \frac{\beta}{\beta + 1} \qquad \beta = \frac{\alpha}{\alpha - 1}$$

Relationship Between Currents

$$I_E = I_B + I_c = (\beta + 1) I_B$$

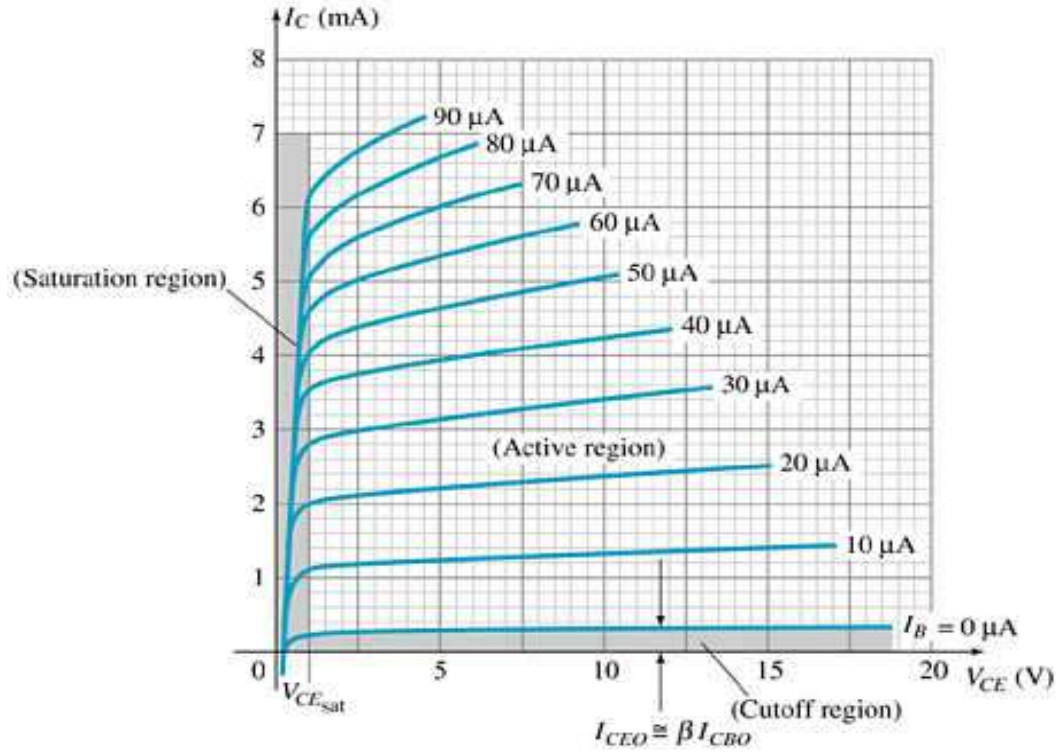
$$\mathbf{I_C = \beta I_B}$$

Common–Collector Configuration



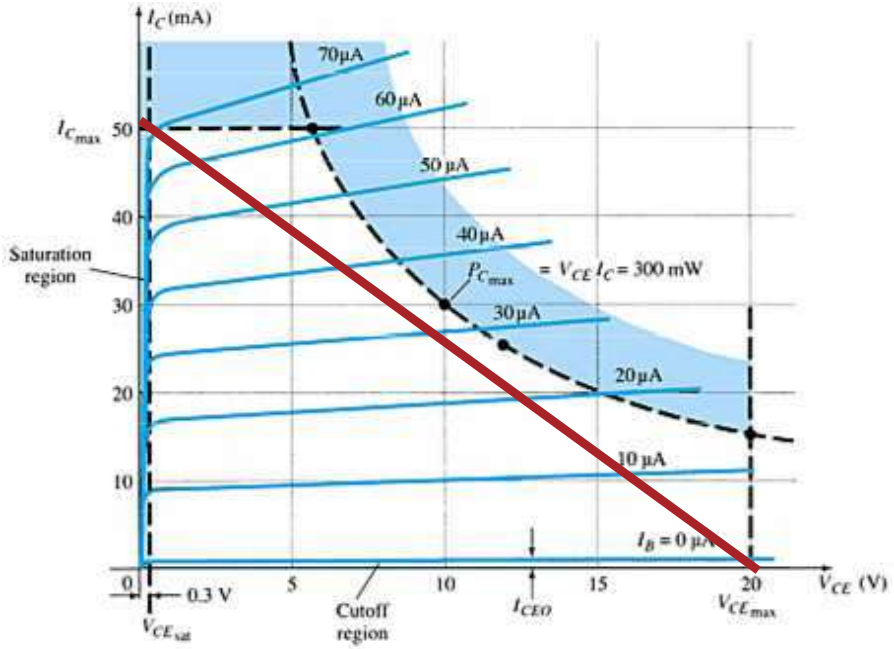
The input is on the base and the output is on the emitter.

Common–Collector Configuration



The characteristics are similar to those of the common-emitter configuration, except the vertical axis is I_E.

Operating Limits for Each Configuration



V_{CE} is at maximum and I_C is at minimum ($I_{Cmax} = I_{CEO}$) in the cutoff region.

I_C is at maximum and V_{CE} is at minimum ($V_{CE\ max} = V_{CEsat} = V_{CEO}$) in the saturation region.

The transistor operates in the active region between saturation and cutoff.

Common-base:

$$P_{Cmax} = V_{CB} I_C$$

Common-emitter:

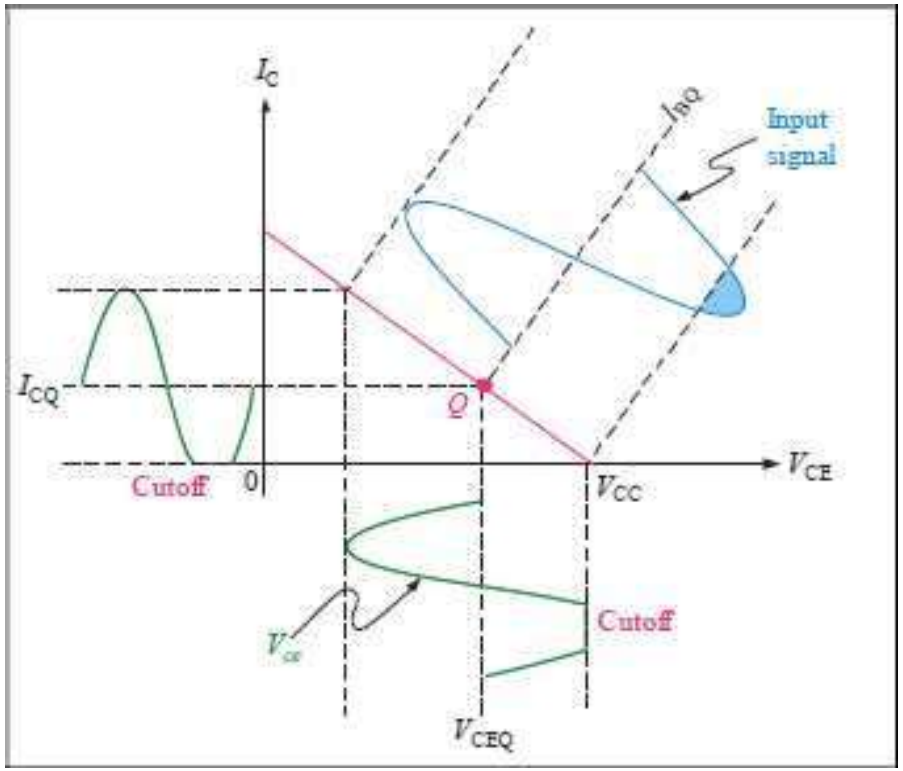
$$P_{Cmax} = V_{CE} I_C$$

Common-collector:

$$P_{Cmax} = V_{CE} I_E$$

Biasing

Biasing: The DC voltages applied to a transistor in order to turn it on so that it can amplify the AC signal.

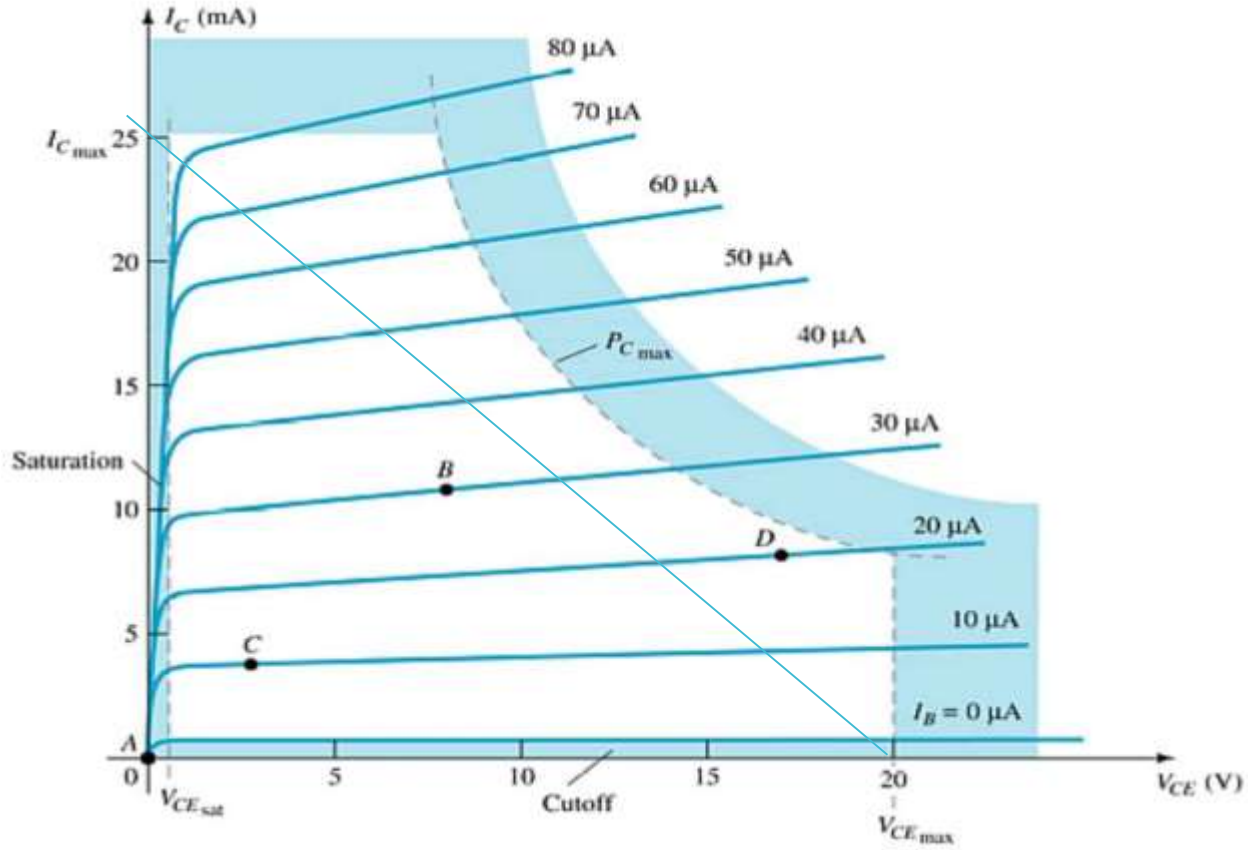


$$V_{BE} = 0.7\,V$$

$$I_E = (\beta + 1) I_B \cong I_C$$

$$I_C = \beta I_B$$

Operating Point



The DC input establishes an operating or *quiescent point* called the *Q-point*.

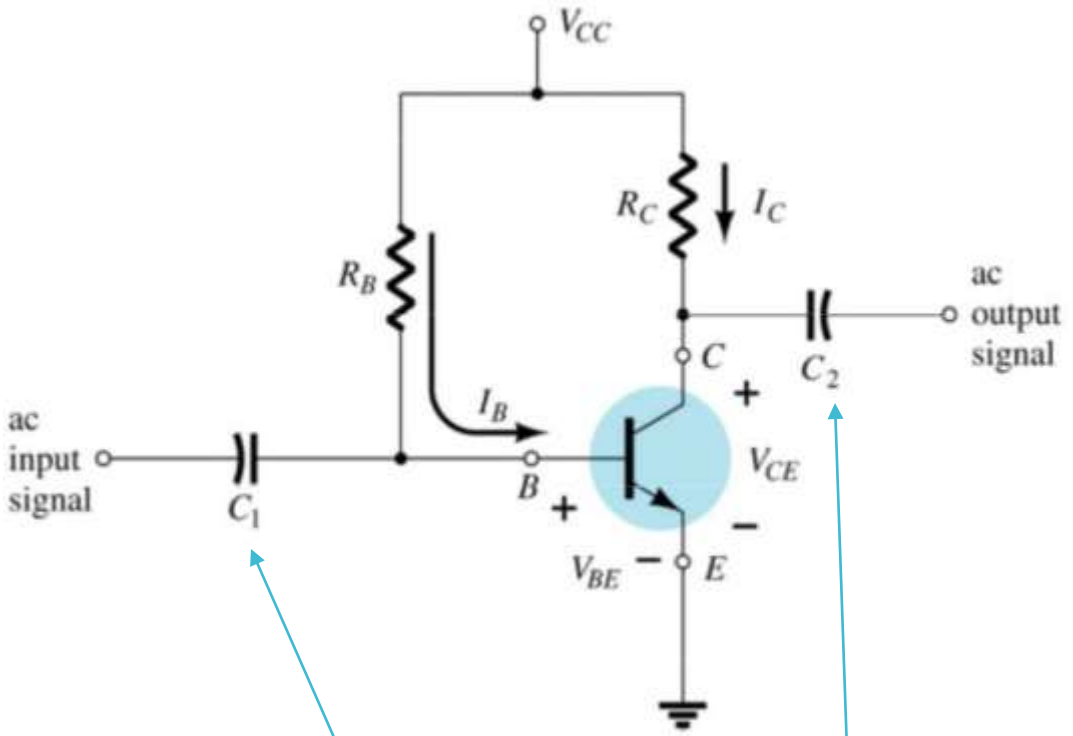
The Three States of Operation

- Active or Linear Region Operation Base–Emitter junction is forward biased Base–Collector junction is reverse biased

- Cutoff Region Operation
  Base–Emitter junction is reverse biased

- Saturation Region Operation
  Base–Emitter junction is forward biased Base–Collector junction is forward biased

Fixed Bias



Πυκνωτής Σύζευξης

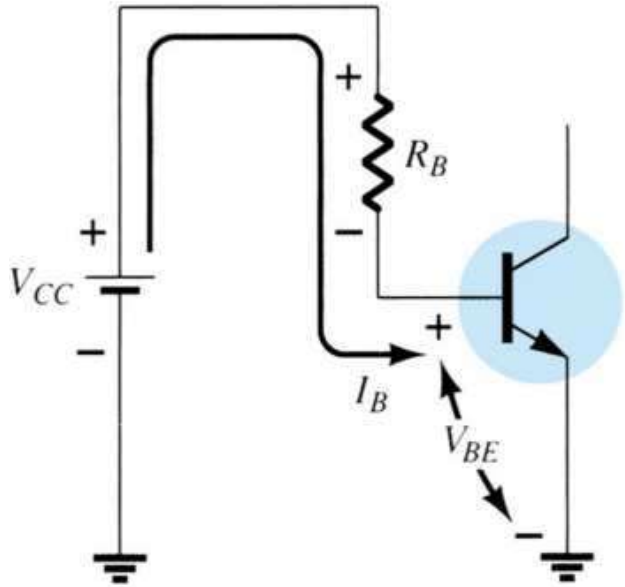
The Base-Emitter Loop

From Kirchhoff's voltage law:

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

Solving for base current:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$



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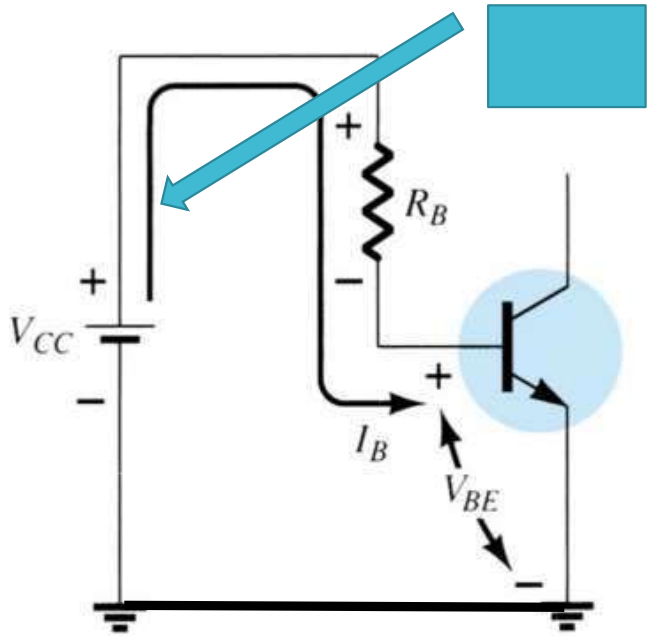


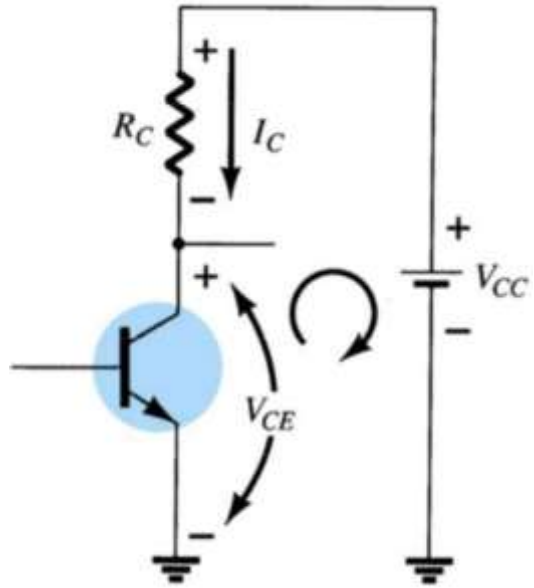
Collector-Emitter Loop

Collector current:

$$I_C = \beta I_B$$

From Kirchhoff's voltage law:

$$V_{CE} = V_{CC} - I_C R_C$$



Collector-Emitter Loop

Collector current:

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From Kirchhoff's voltage law:

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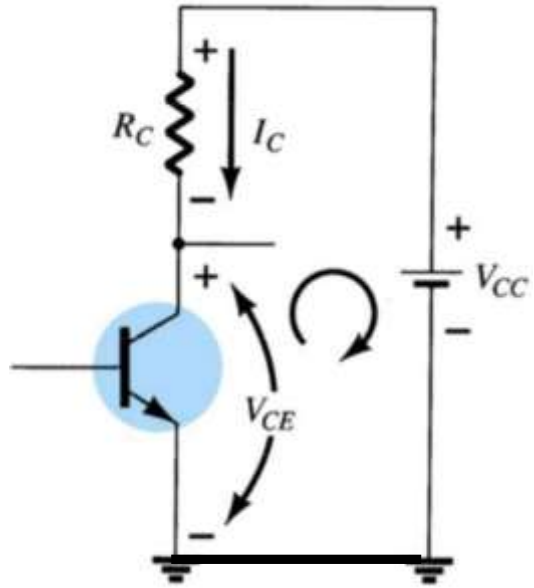


Saturation

When the transistor is operating in saturation, current through the transistor is at its *maximum* possible value.

$$I_{Csat} = \frac{V_{CC}}{R_C}$$

$$V_{CE} \cong 0\,V$$

This approximation is equivalent to move the region below V_{CEsat} of the output curves to align on the output current axis.

Load Line Analysis

The end points of the load line are:

I_{Csat}

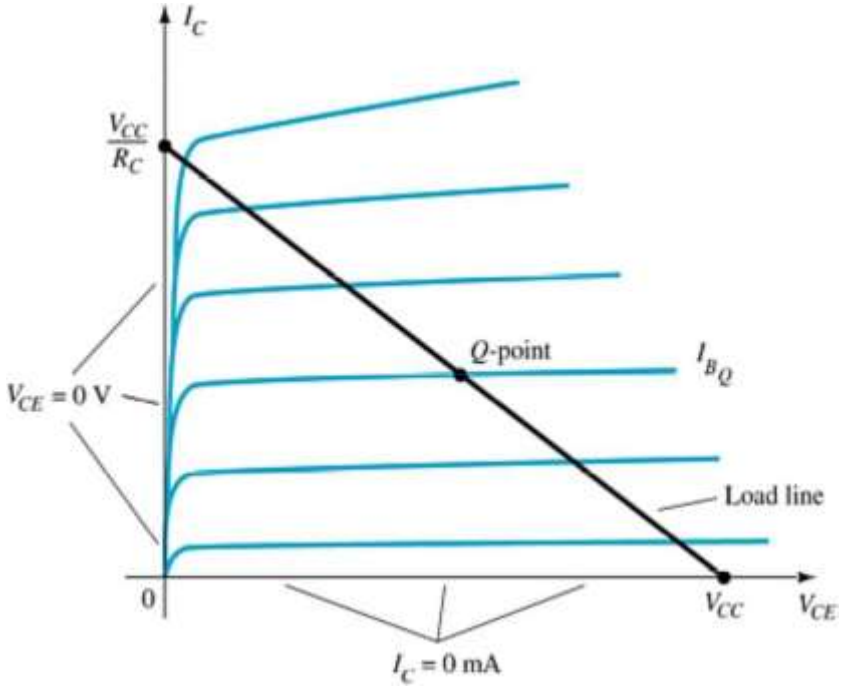
$I_C = V_{CC} / R_C$

$V_{CE} = 0\ V$

$V_{CEcutoff}$

$V_{CE} = V_{CC}$

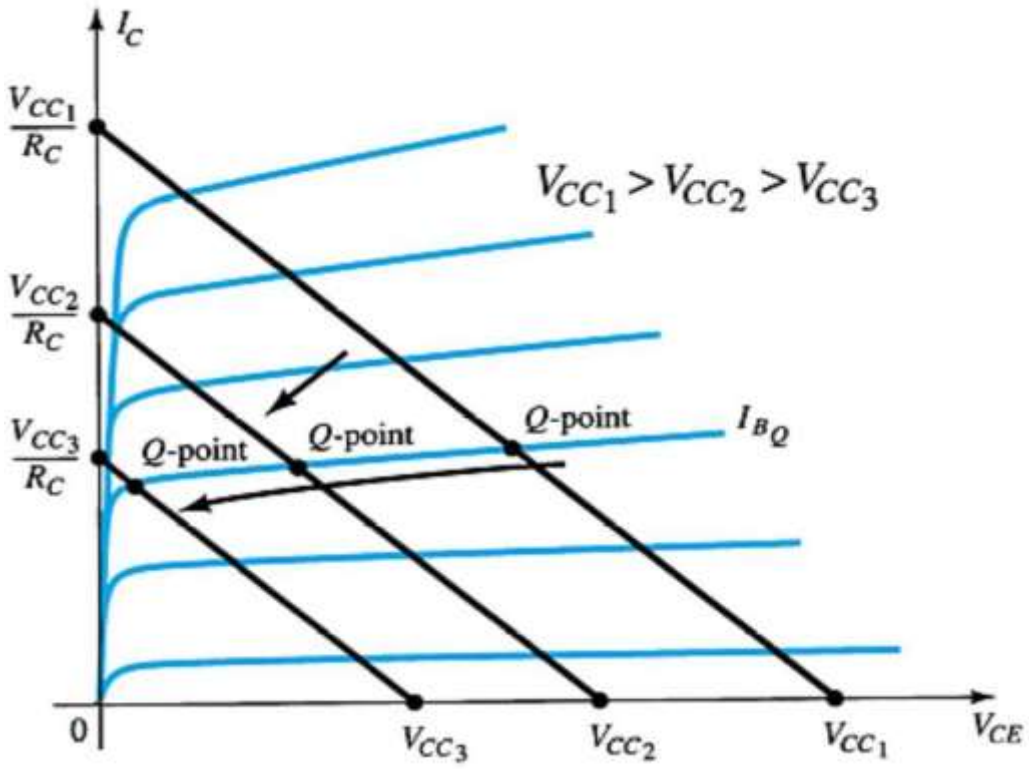
$I_C = 0\ mA$



The Q-point is the operating point:

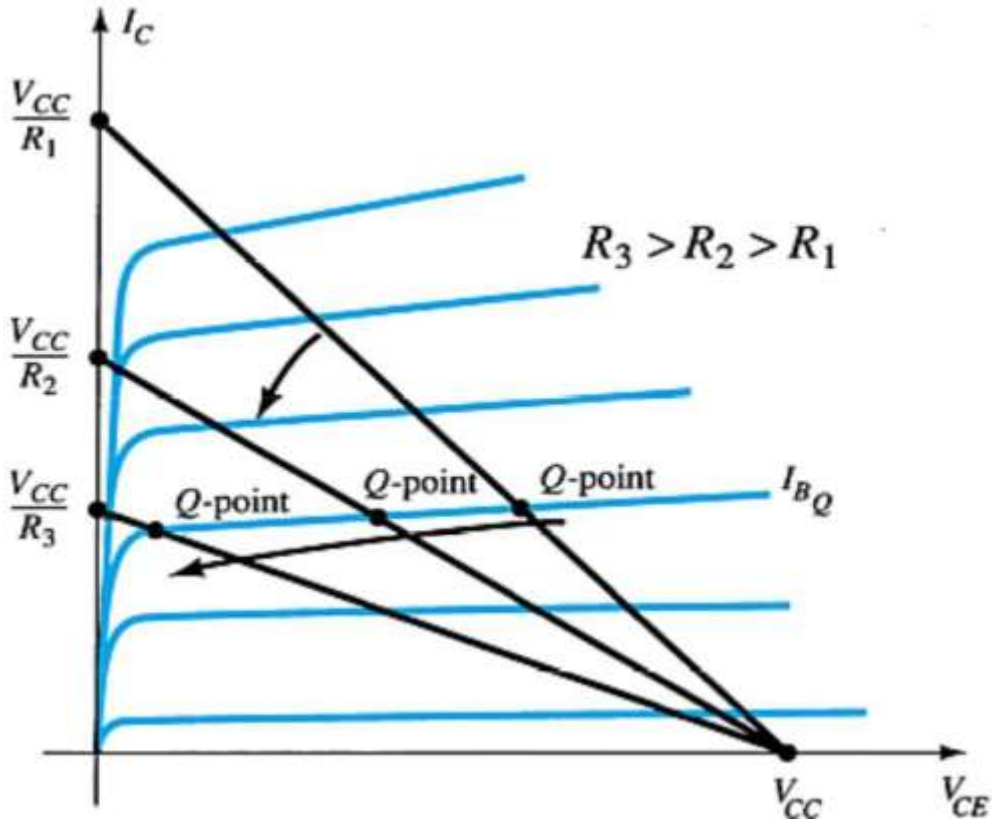
- where the value of R_B sets the value of I_B
- that sets the values of V_{CE} and I_C

Circuit Values Affect the Q-Point



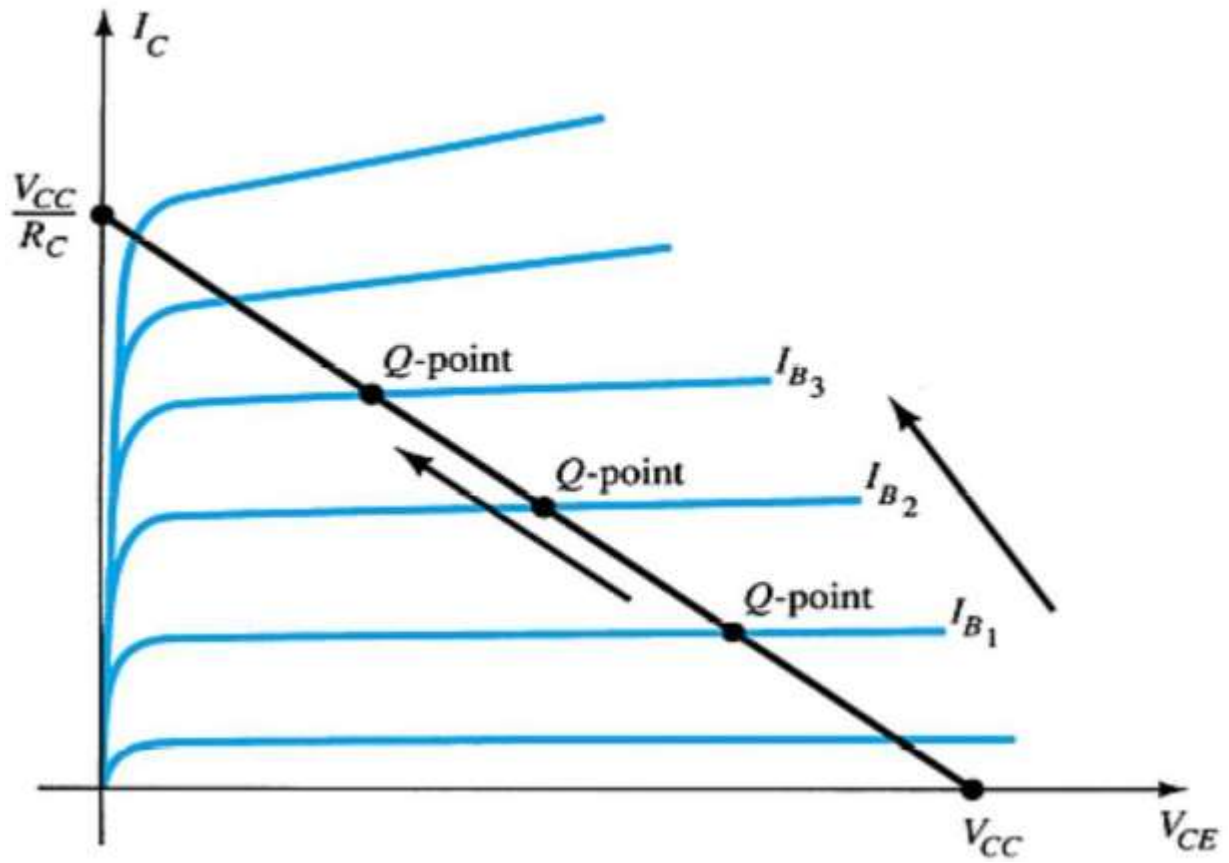
more …

Circuit Values Affect the Q-Point



more …

Circuit Values Affect the Q-Point



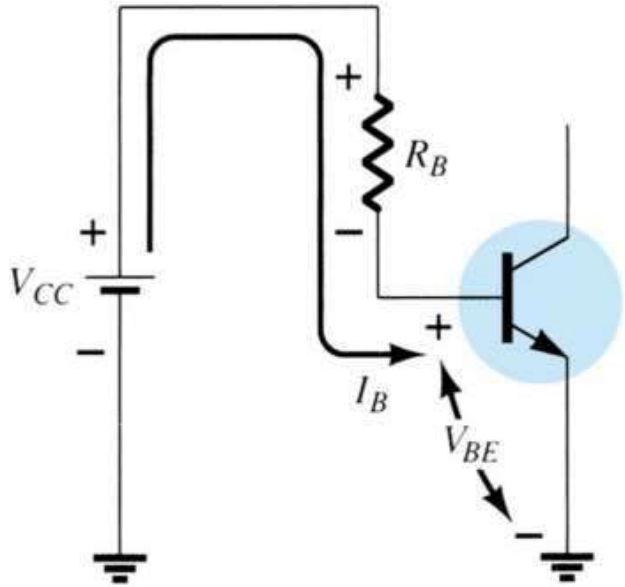
(υπενθύμιση) The Base-Emitter Loop

From Kirchhoff's voltage law:

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

Solving for base current:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$



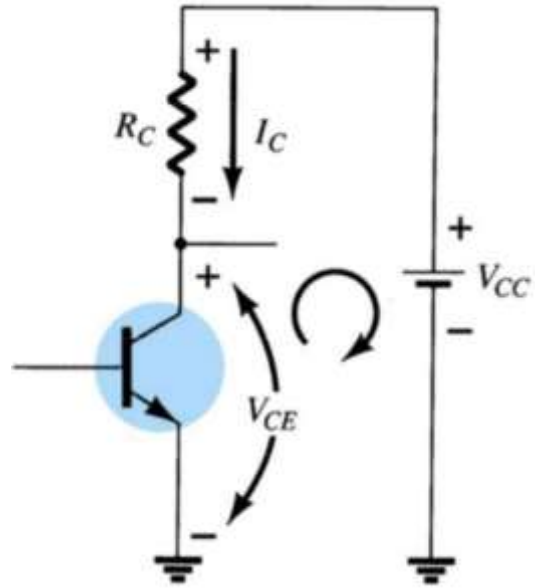
(υπενθύμιση) Collector-Emitter Loop

Collector current:

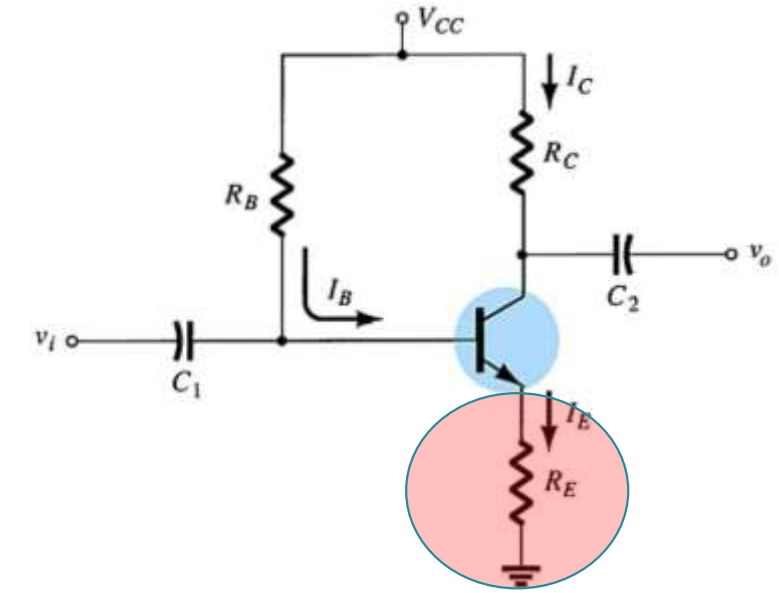
$$I_C = \beta I_B$$

From Kirchhoff's voltage law:

$$V_{CE} = V_{CC} - I_C R_C$$



Emitter-Stabilized Bias Circuit



Adding a resistor (R_E) to the emitter circuit stabilizes the bias circuit.

Base-Emitter Loop

From Kirchhoff's voltage law:

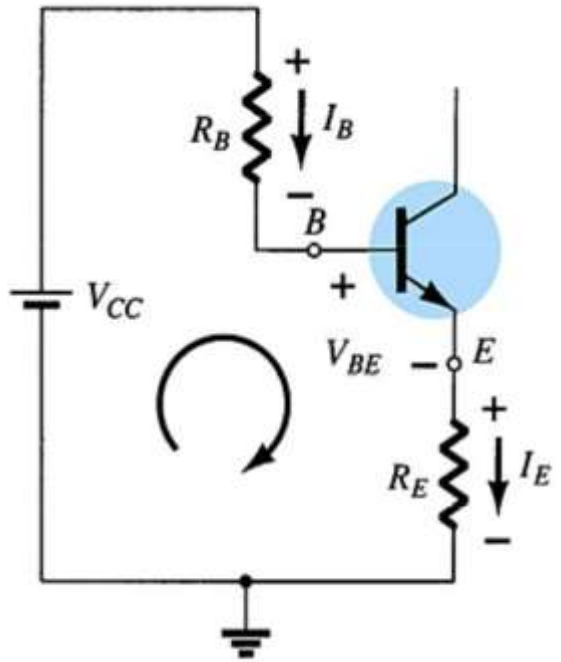
$$+ V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

Since $I_E = (\beta + 1) I_B$:

$$V_{CC} - I_B R_B - V_{BE} - (\beta + 1) I_B R_E = 0$$

Solving for I_B:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}$$



Collector-Emitter Loop

From Kirchhoff's voltage law:

$$I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Since $I_E \cong I_C$:

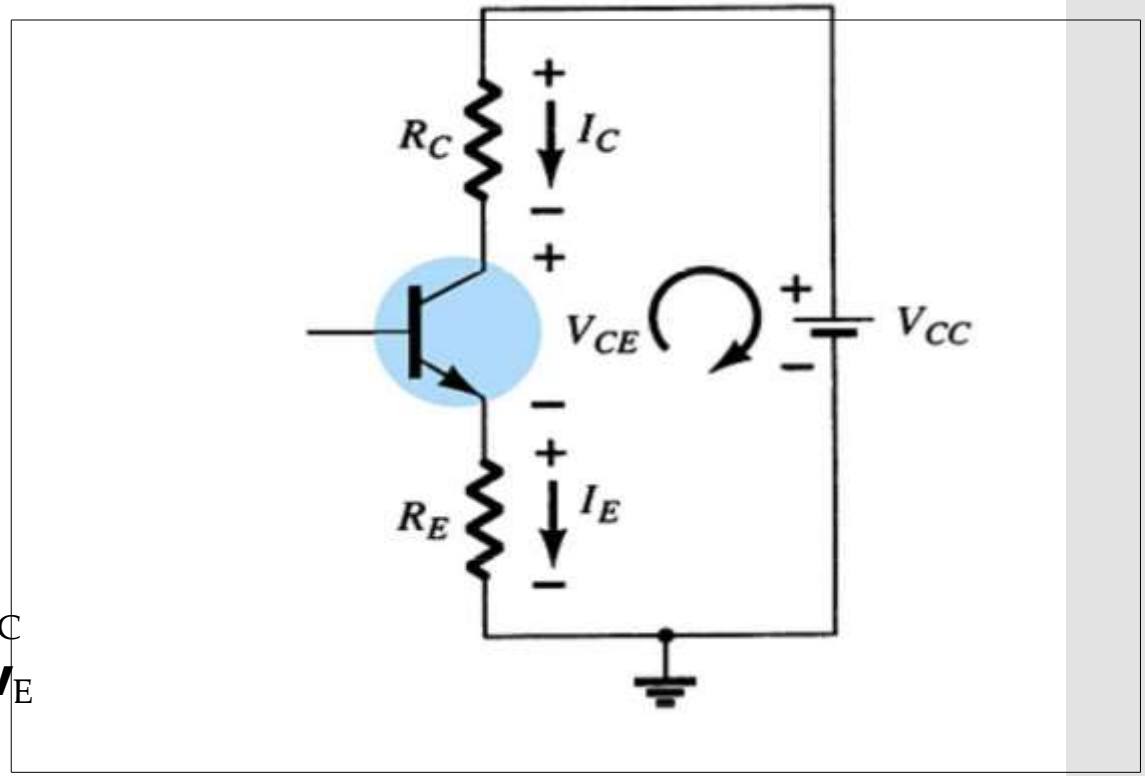
$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Also:

$$V_E = I_E R_E$$

$$V_C = V_{CE} + V_E = V_{CC} - I_C R_C$$

$$V_B = V_{CC} - I_R R_B = V_{BE} + V_E$$



Improved Biased Stability

Stability refers to a circuit condition in which the currents and voltages will remain fairly constant over a wide range of temperatures and transistor Beta (β) values.

Adding RE to the emitter improves the stability of a transistor.

Fixed-bias circuit

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

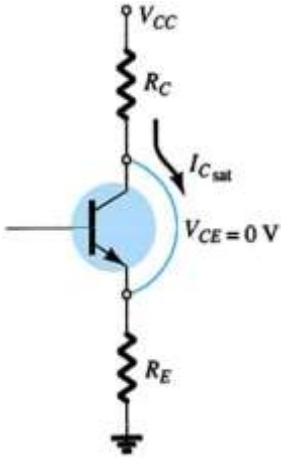
Emitter-stabilized bias circuit

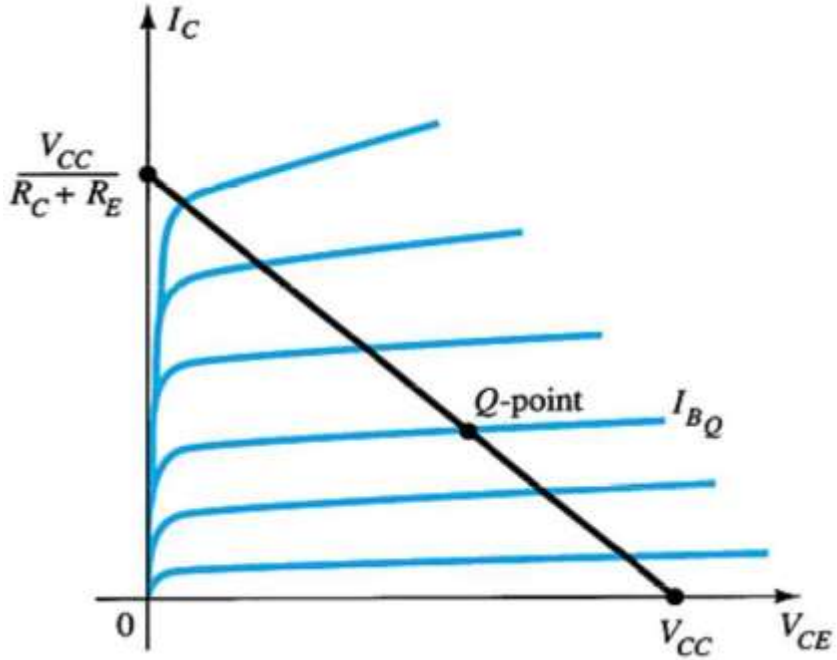
$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

$$I_C = \beta I_B$$

I_B in fixed-bias circuit cannot change, so change in β results in large change in output current and voltage.

Saturation Level





The endpoints can be determined from the load line.

$V_{CEcutoff}$:

$V_{CE} = V_{CC}$

$I_C = 0mA$

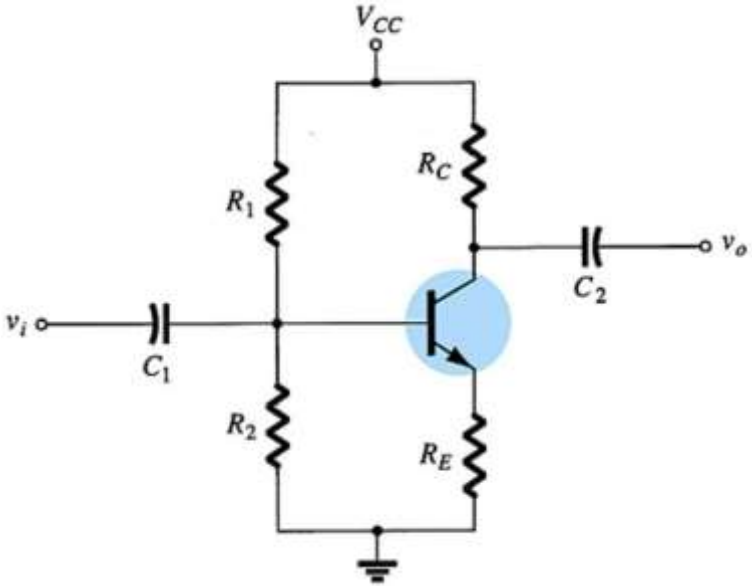
I_{Csat}: $V_{CE} = 0V$

$$I_C = \frac{V_{CC}}{R_C + R_E}$$

Voltage Divider Bias

This is a very stable bias circuit.

The currents and voltages are nearly independent of any variations in β.



Approximate Analysis

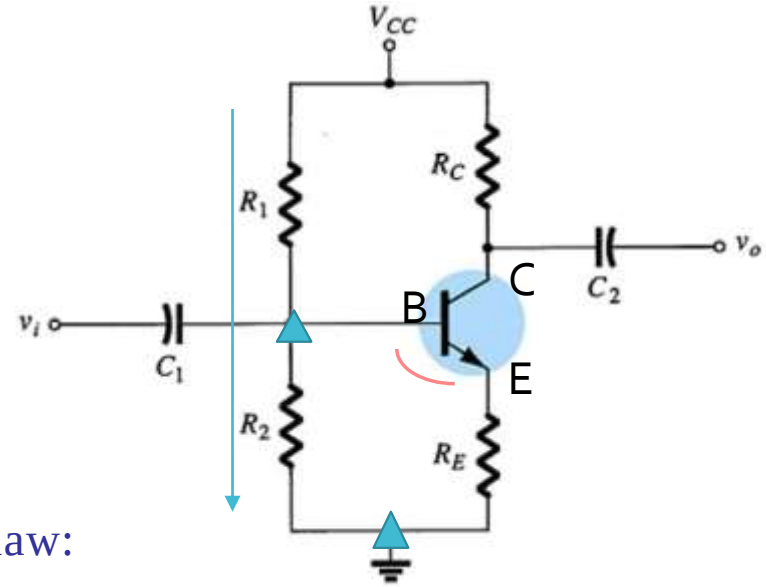
Where $I_B << I_1$ and $I_1 \cong I_2$: (Διαιρέτης τάσης)

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

Where $\beta R_E > 10R_2$:

$$I_E = \frac{V_E}{R_E}$$

$$V_E = V_B - V_{BE}$$



From Kirchhoff's voltage law:

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$I_E \cong I_C$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Διαιρέτης τάσης Voltage Divider Bias Analysis

Transistor Saturation Level

$$I_{Csat} = I_{Cmax} = \frac{V_{CC}}{R_C + R_E}$$

Load Line Analysis

Cutoff:

$V_{CE} = V_{CC}$

$I_C = 0mA$

Saturation:

$$I_C = \frac{V_{CC}}{R_C + R_E}$$

$V_{CE} = 0V$

Voltage Divider Bias

$$V_B = \left(\frac{R_2}{R_1 + R_2}\right) V_{CC}$$

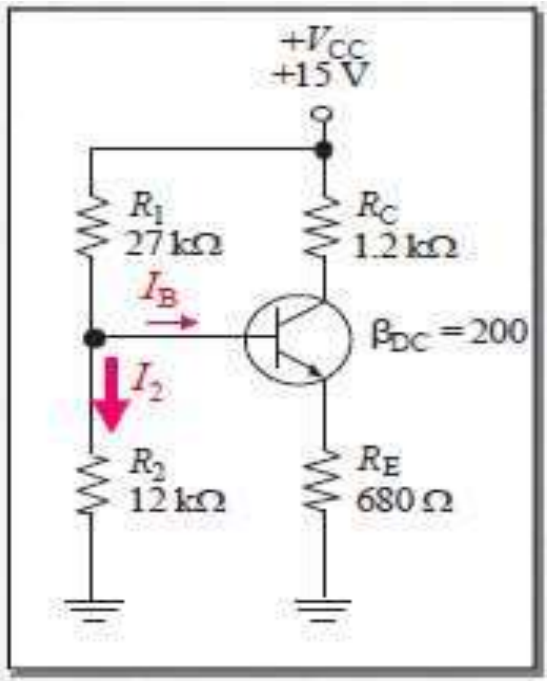
$$= \left(\frac{12\ \text{k}\Omega}{27\ \text{k}\Omega + 12\ \text{k}\Omega}\right)(+15\ \text{V}) = 4.62\ \text{V}$$

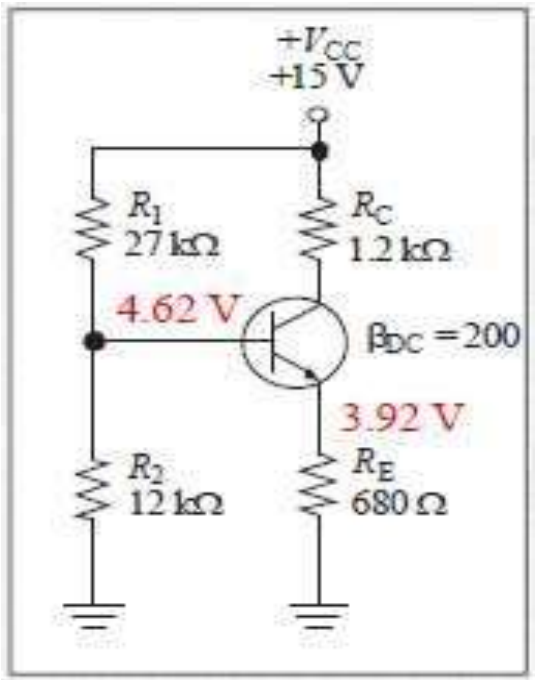
V_E is one diode drop less than V_B:

$$V_E = 4.62\ \text{V} - 0.7\ \text{V} = 3.92\ \text{V}$$

Applying Ohm's law:

$$I_E = \frac{V_E}{R_E} = \frac{3.92\ \text{V}}{680\ \Omega} = 5.76\ \text{mA}$$





Voltage Divider Bias (Exact)

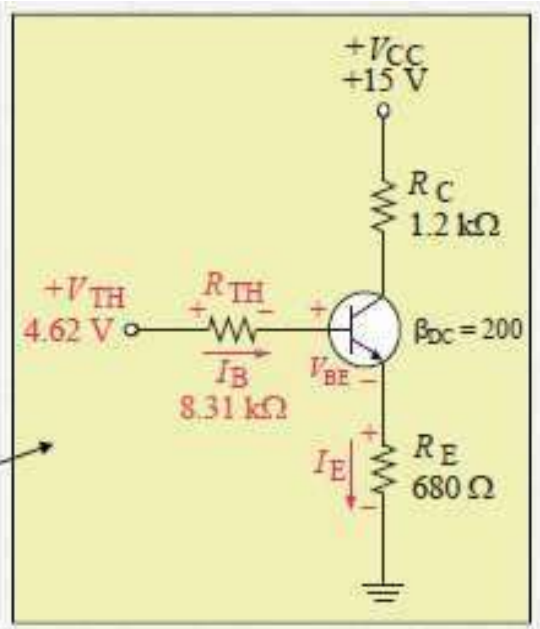
$V_{TH} = V_{B(\text{no load})}$

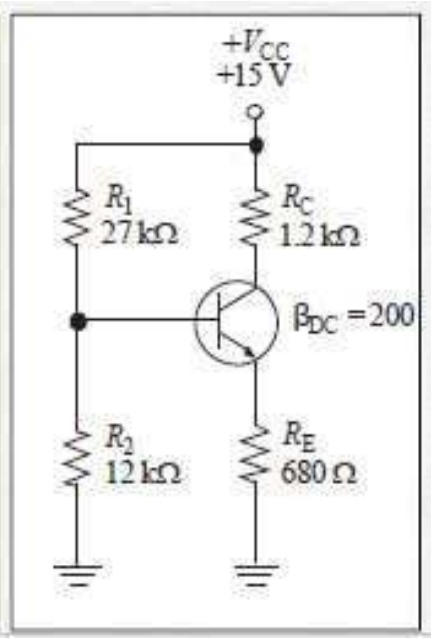
$= 4.62\ \text{V}$

$R_{TH} = R_1 \| R_2 =$

$= 8.31\ \text{k}\Omega$

The Thevenin input circuit can be drawn





$V_{TH} = I_B R_{TH} + V_{BE} + I_E R_E$

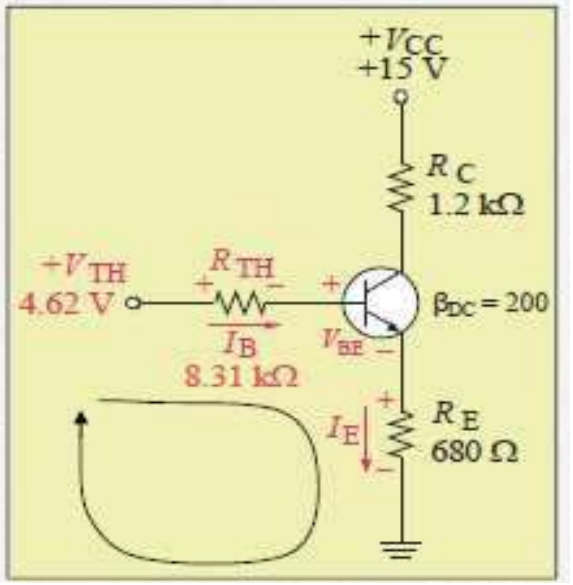
$$I_E = \frac{V_{TH} - V_{BE}}{R_E + R_{TH}/\beta_{DC}}$$

Substituting and solving,

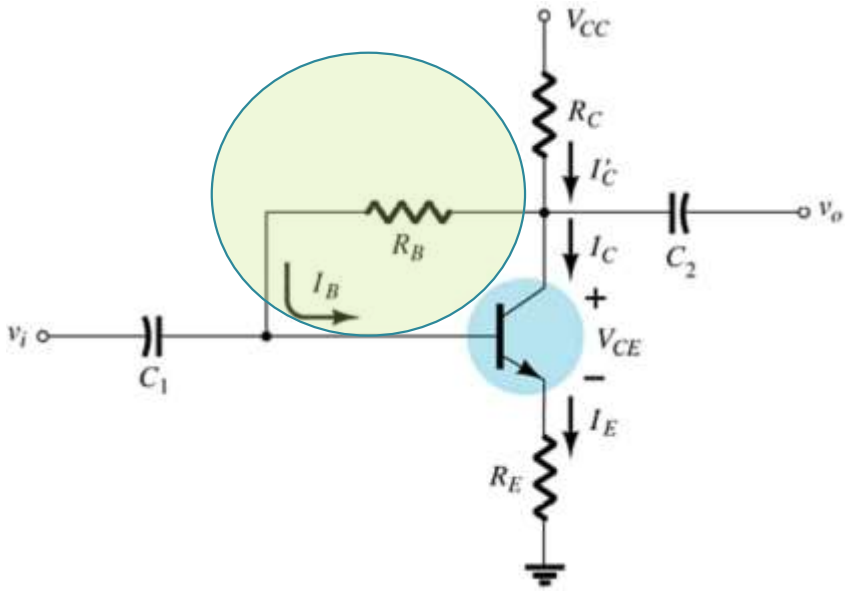
$$I_E = \frac{4.62\ \text{V} - 0.7\ \text{V}}{680\ \Omega + 8.31\ \text{k}\Omega/200} = 5.43\ \text{mA}$$

and $V_E = I_E R_E = (5.43\ \text{mA})(0.68\ \text{k}\Omega)$

$= 3.69\ \text{V}$



DC Bias with Voltage Feedback



Another way to improve the stability of a bias circuit is to add a feedback path from collector to base.

In this bias circuit the Q-point is only slightly dependent on the transistor beta, β.

Base-Emitter Loop

From Kirchhoff's voltage law:

$$V_{CC} - I'_C R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

Where $I_B << I_C$:

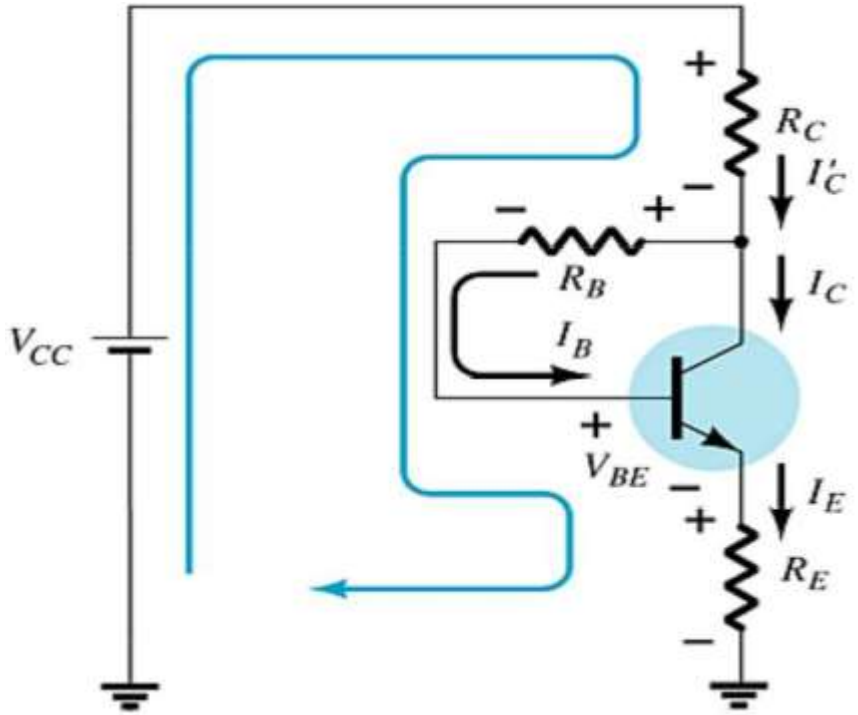
$$I'_C = I_C + I_B \cong I_C$$

Knowing $I_C = \beta I_B$ and $I_E \cong I_C$, the loop equation becomes:

$$V_{CC} - \beta I_B R_C - I_B R_B - V_{BE} - \beta I_B R_E = 0$$

Λύνοντας ως προς I_B:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$



Εφαρμόζοντας τον KVL:

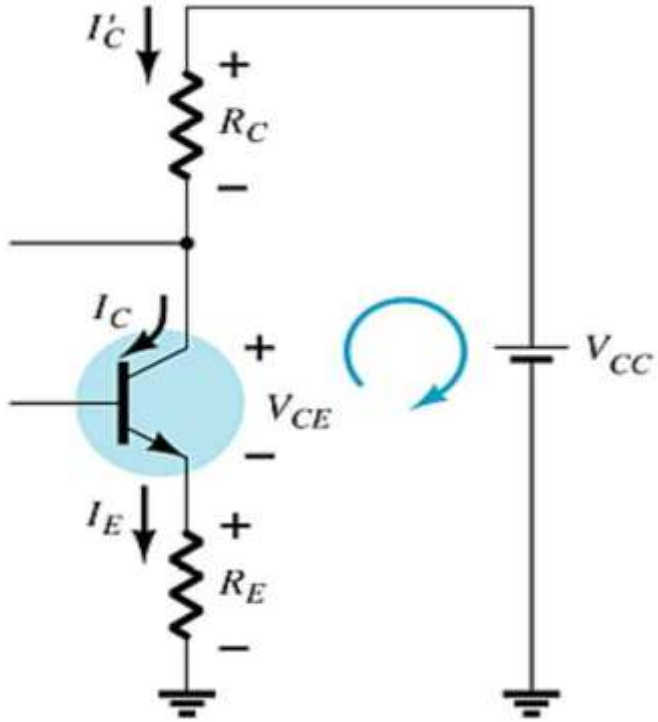
$$I_E + V_{CE} + I'_C R_C - V_{CC} = 0$$

Since $I'_C \cong I_C$ and $I_C = \beta I_B$:

$$I_C(R_C + R_E) + V_{CE} - V_{CC} = 0$$

Λύνοντας ως προς V_{CE} έχουμε:

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$



END of Part A