



ΠΑΝΕΠΙΣΤΗΜΙΟ ΔΥΤΙΚΗΣ ΑΤΤΙΚΗΣ

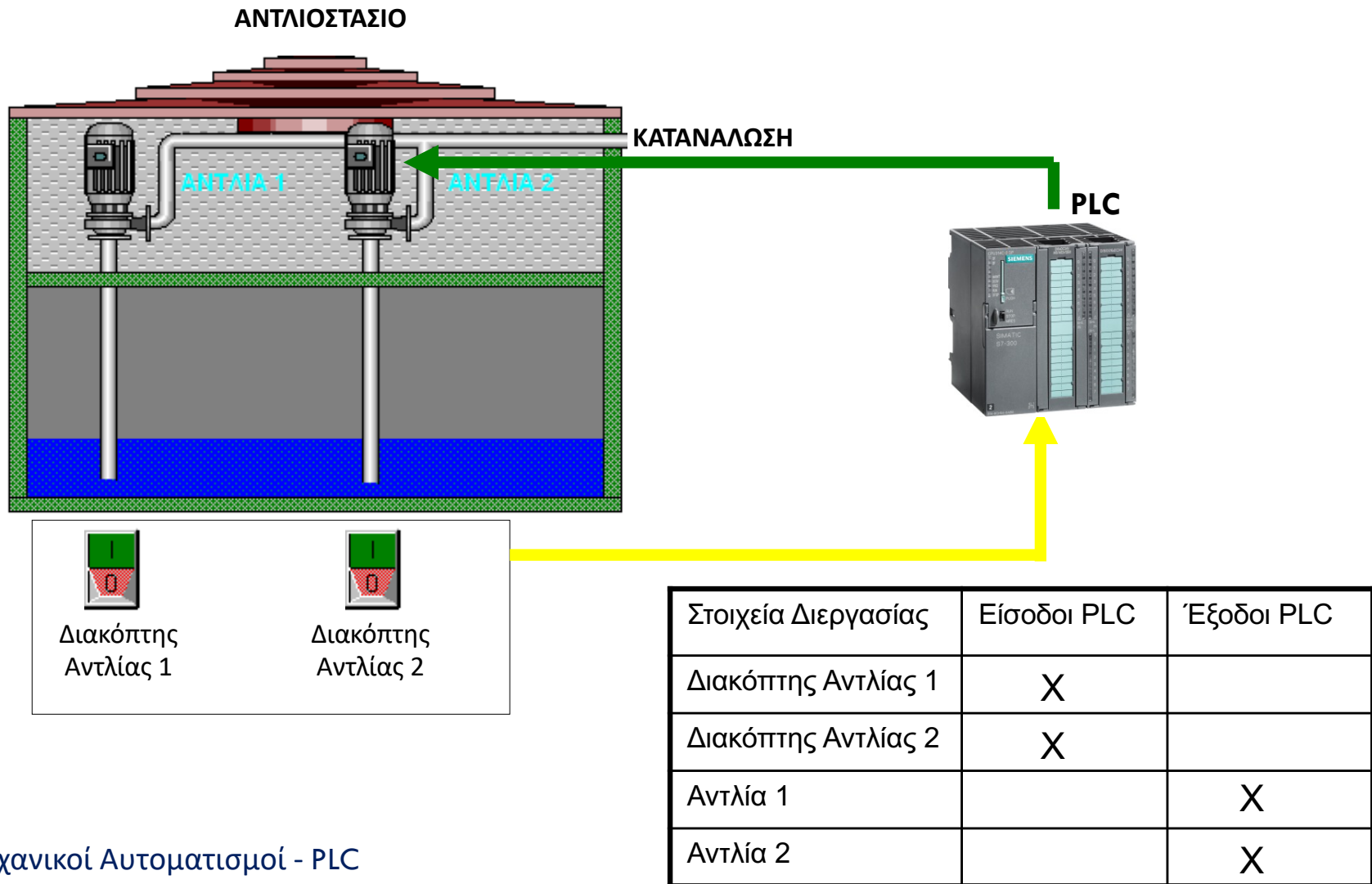
Σχολή Μηχανικών

Τμήμα Μηχανικών Βιομηχανικής Σχεδίασης και Παραγωγής

# Βιομηχανικοί Αυτοματισμοί - PLC

Θεοχάρης Ευστάθιος

## ΔΙΕΡΓΑΣΙΑ



## ΕΠΙΣΚΟΠΗΣΗ



HMI

CONTROLLER



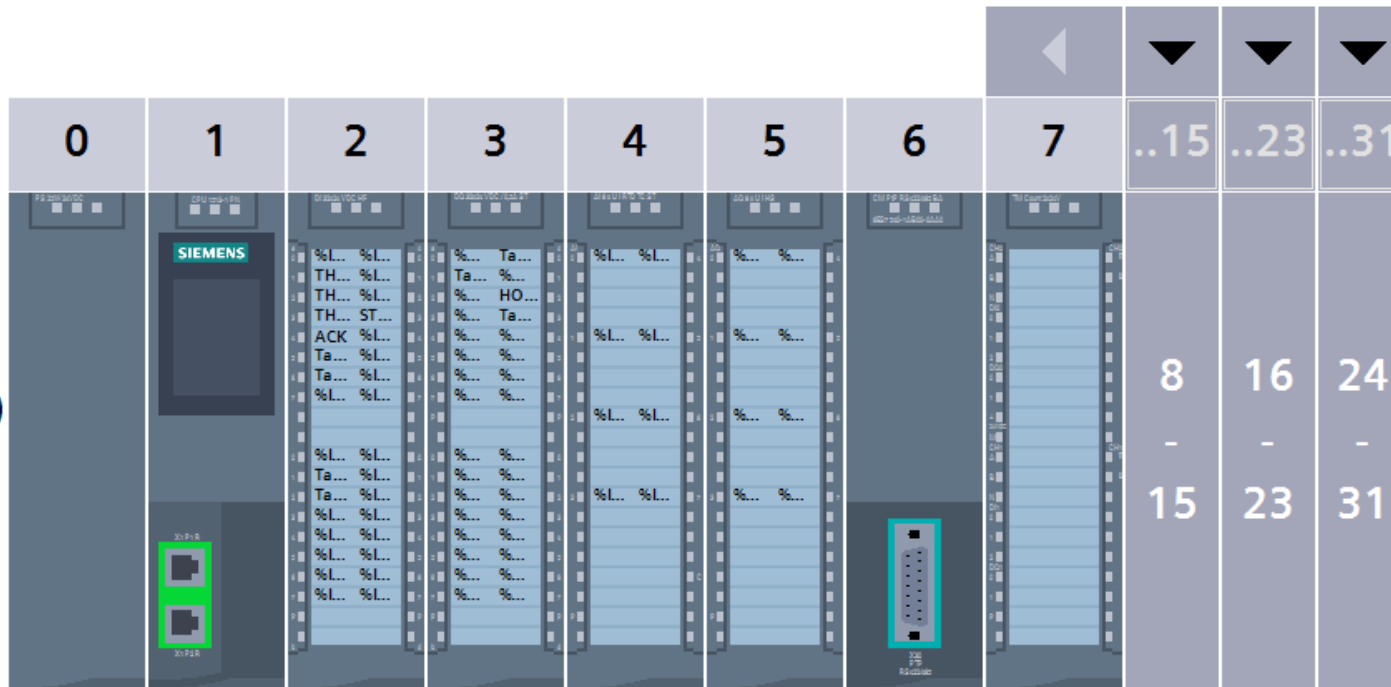
I/O

- ETHERNET
- PROFIBUS, MODBUS, CANBUS
- AS-I

## PLC - ΚΑΤΗΓΟΡΙΕΣ ΚΑΡΤΩΝ

PS 25W 24VD...  
 CPU  
 DI 32x24VDC...  
 DQ 32x24VDC...  
 AI 8xUI/RTD/I...  
 AQ 8xUI/HS\_1  
 CM PtP RS422...  
 TM Count 2x2...

Rail\_0



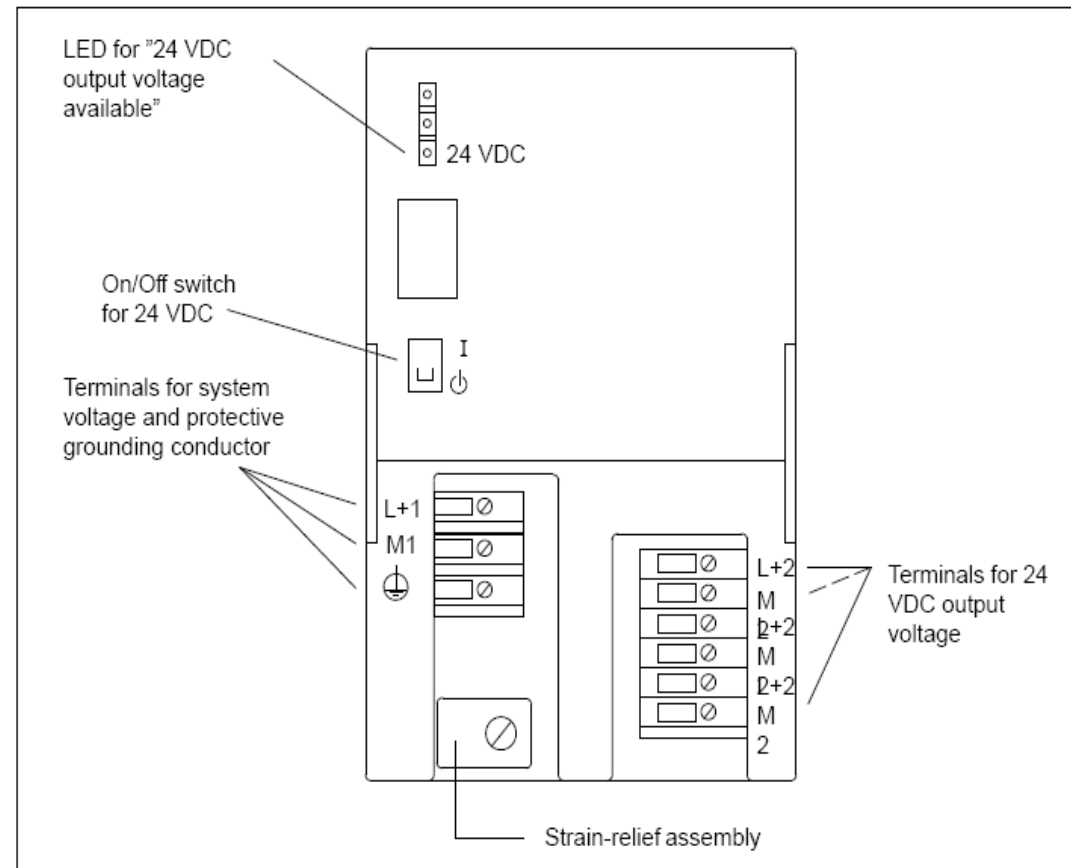


## PLC - ΚΑΤΗΓΟΡΙΕΣ ΚΑΡΤΩΝ

- ❑ **RACK** : Ράγα στήριξης
- ❑ **PS** (Power Supply) : Τροφοδοτικό
- ❑ **CPU** : Κεντρική Μονάδα (επεξεργαστής)
- ❑ **SM** (Signal Module) : Κάρτα Σημάτων
  - ❑ Εισόδων : Ψηφιακών, Αναλογικών
  - ❑ Εξόδων : Ψηφιακών, Αναλογικών
- ❑ **CM** (ή **CP**) : Κάρτα Επικοινωνίας
- ❑ **TM** (ή **FM**) : Κάρτα για PID, Positioning, CAM, Counting, κλπ

## ΤΡΟΦΟΔΟΤΙΚΟ

Wiring schematic of the PS 305; 2 A



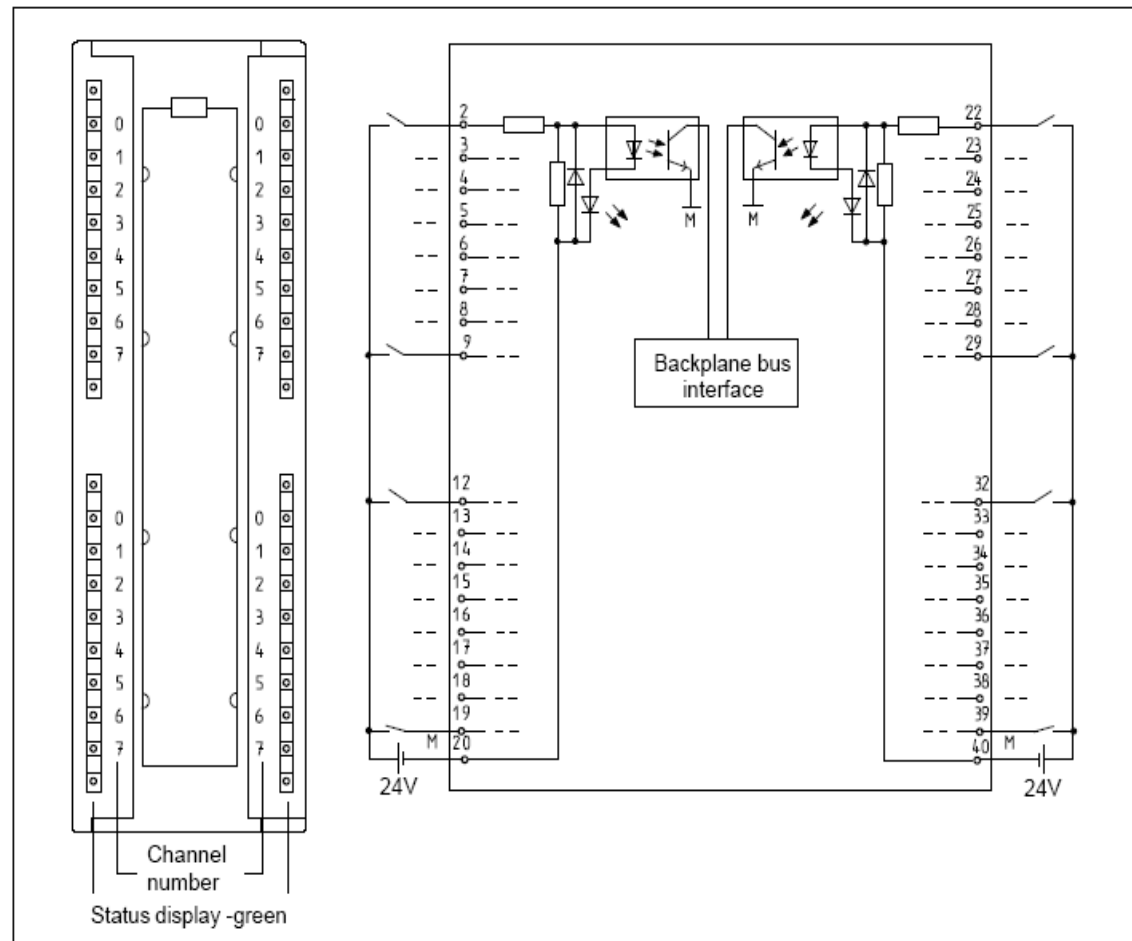
Wiring Schematic of the PS 305 Power Supply Module (2 A)

## CPU



## DI – ΨΗΦΙΑΚΟΙ ΕΙΣΟΔΟΙ

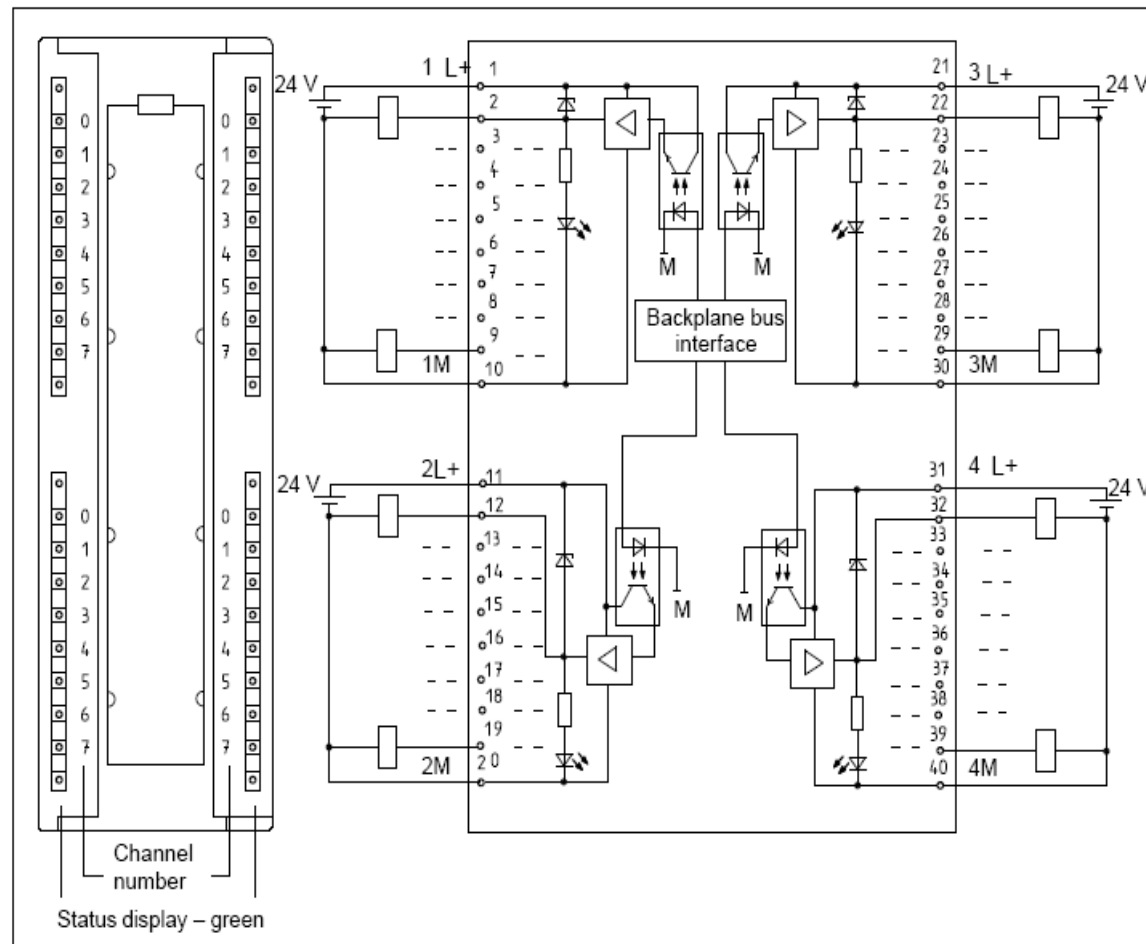
Terminal assignment and block diagram of the SM 321; DI 32 × 24 VDC





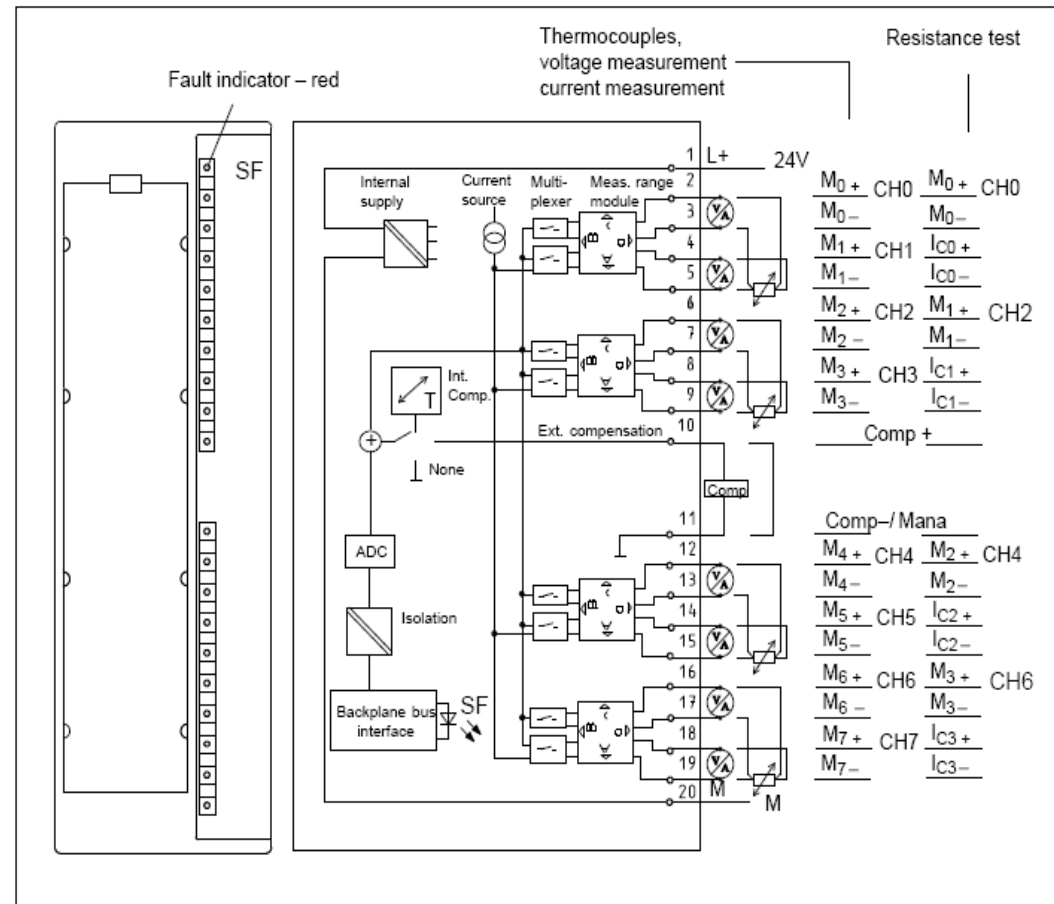
## DO – ΨΗΦΙΑΚΕΣ ΕΞΟΔΟΙ

Module View and Block Diagram of the SM 322; DO 32 × 24 VDC/ 0.5 A



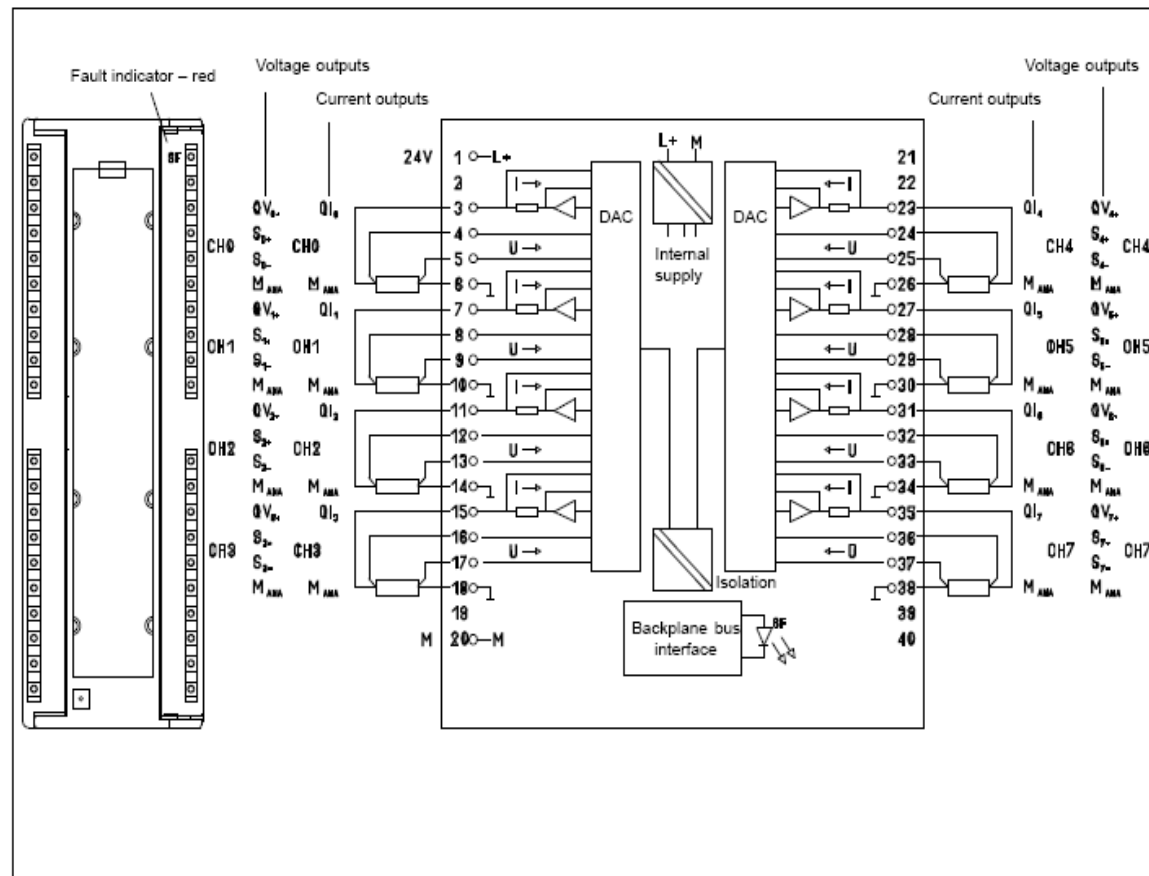
## ΑΙ – ΑΝΑΛΟΓΙΚΕΣ ΕΙΣΟΔΟΙ

Terminal connection diagram and block diagram of the SM 331; AI 8 × 12 bits



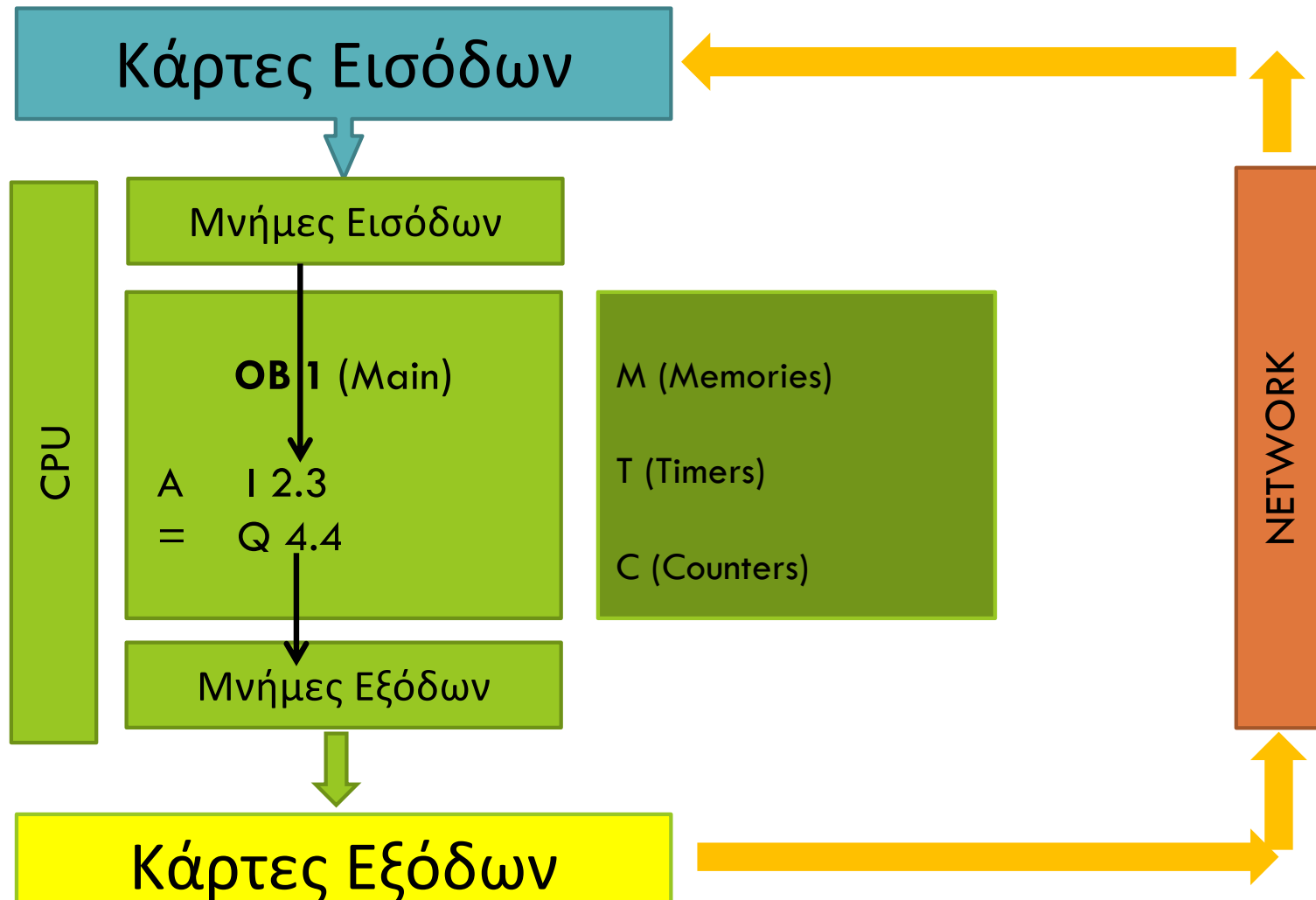
## ΑΟ – ΑΝΑΛΟΓΙΚΕΣ ΕΞΟΔΟΙ

Terminal connection and block diagram of analog output module SM 332;  
AO 8 × 12 bits

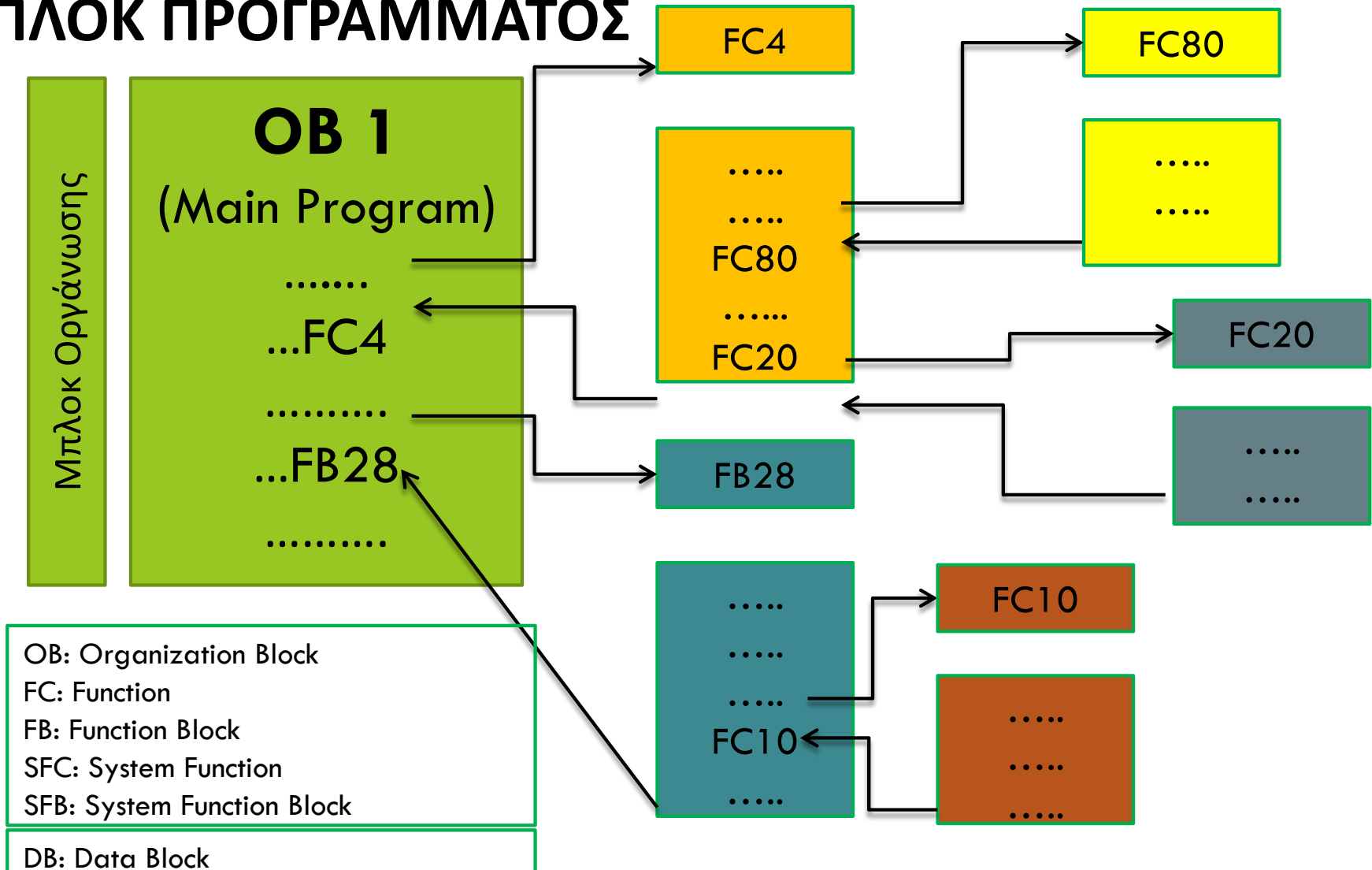




# ΚΥΚΛΙΚΗ ΕΠΕΞΕΡΓΑΣΙΑ (ΚΥΚΛΟΣ ΠΡΟΓΡΑΜΜΑΤΟΣ P L C)



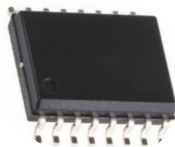
## ΜΠΛΟΚ ΠΡΟΓΡΑΜΜΑΤΟΣ



## PLC MEMORIES

LOAD MEMORY	WORK MEMORY	RETAIN MEMORY
RAM EPROM EEPROM	RAM	EEPROM

RAM



EPROM



EEPROM



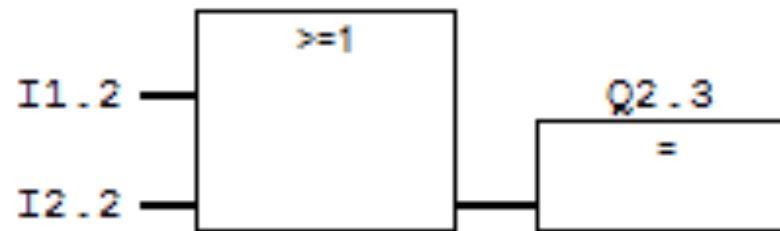
## ΛΟΓΙΚΗ ΕΝΤΟΛΗ : OR

ΛΟΓΙΚΟΣ ΠΙΝΑΚΑΣ		
I1.2	I2.2	Q2.3
0	0	0
0	1	1
1	0	1
1	1	1

LAD



FBD



STL

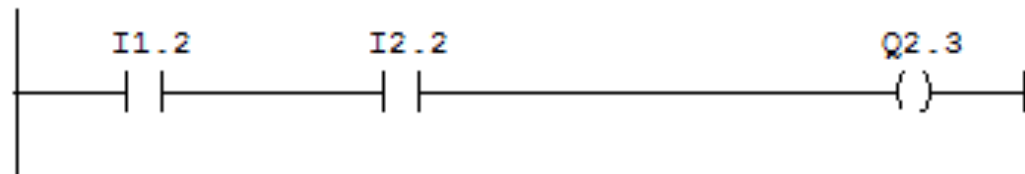
```

O      I      1.2
O      I      2.2
=      Q      2.3
  
```

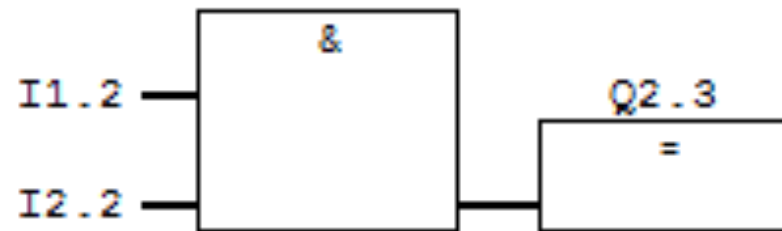
## ΛΟΓΙΚΗ ΕΝΤΟΛΗ : AND

ΛΟΓΙΚΟΣ ΠΙΝΑΚΑΣ		
I1.2	I2.2	Q2.3
0	0	0
0	1	0
1	0	0
1	1	1

LAD



FBD



STL

```

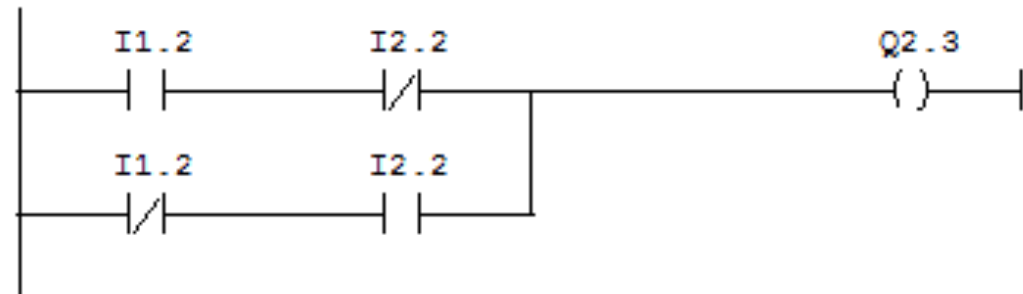
A      I      1.2
A      I      2.2
=      Q      2.3
  
```



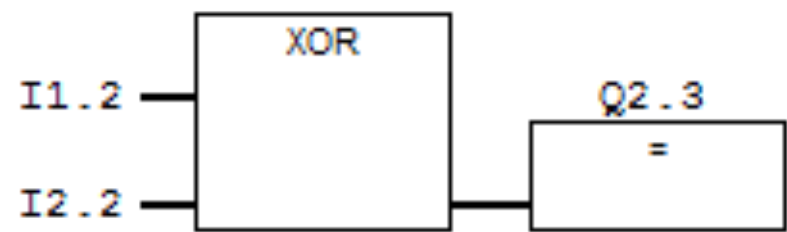
## ΛΟΓΙΚΗ ΕΝΤΟΛΗ : XOR (Exclusive OR)

ΛΟΓΙΚΟΣ ΠΙΝΑΚΑΣ		
I1.2	I2.2	Q2.3
0	0	0
0	1	1
1	0	1
1	1	0

LAD



FBD



STL

```

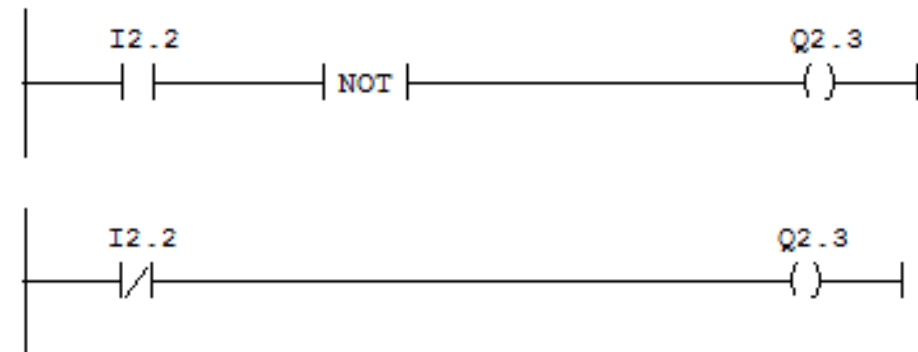
X      I      1.2
X      I      2.2
=      Q      2.3
  
```

## ΛΟΓΙΚΗ ΕΝΤΟΛΗ : NOT

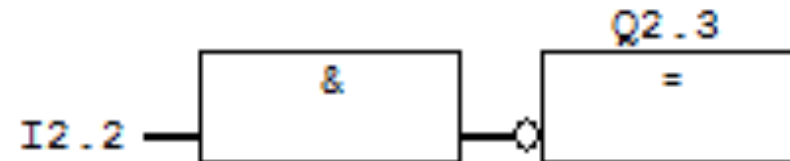
### ΛΟΓΙΚΟΣ ΠΙΝΑΚΑΣ

I2.2	Q2.3
1	0
0	1

LAD



FBD



STL

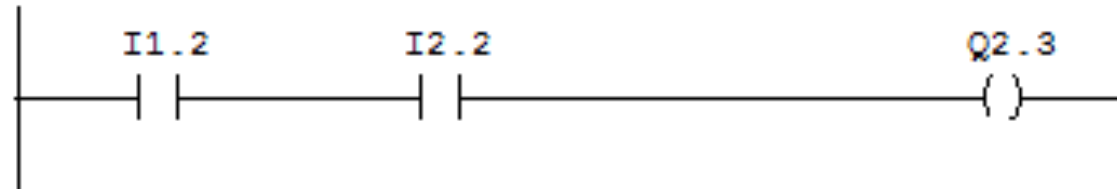
```

AN      I      2.2
=       Q      2.3

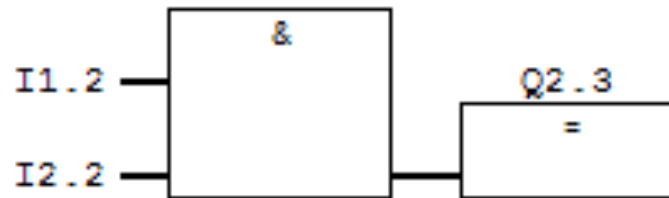
A       I      2.2
NOT    =       Q      2.3
  
```

## ΛΟΓΙΚΗ ΕΝΤΟΛΗ : = (Assignment)

LAD



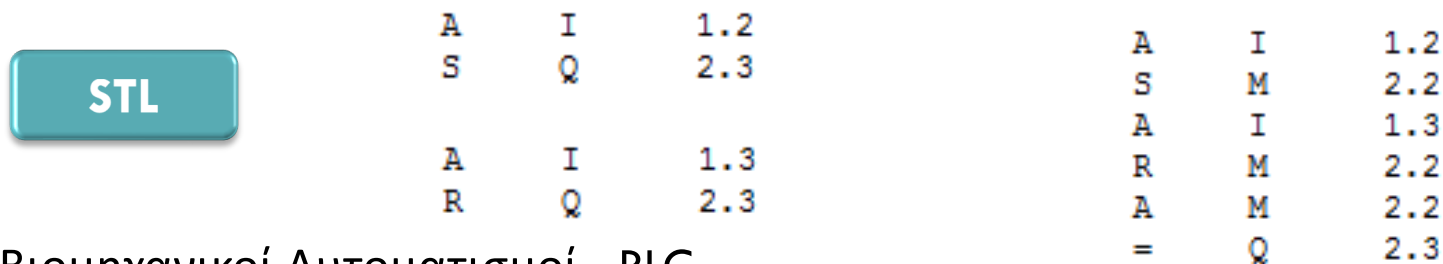
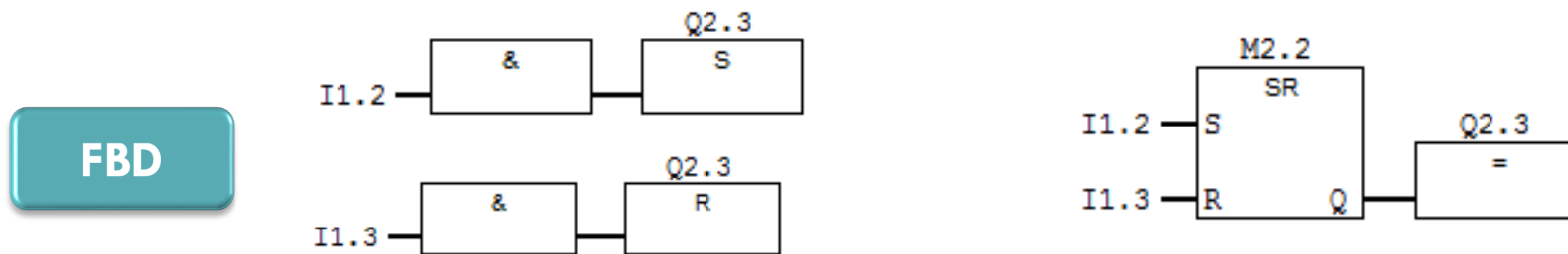
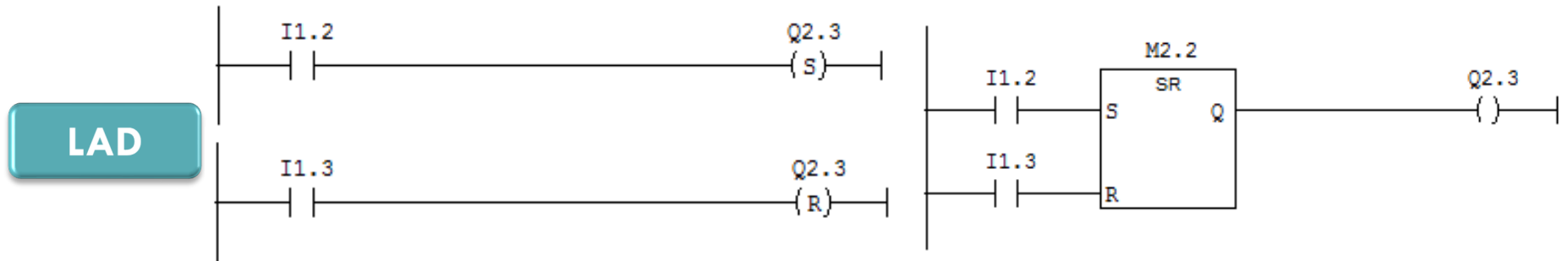
FBD



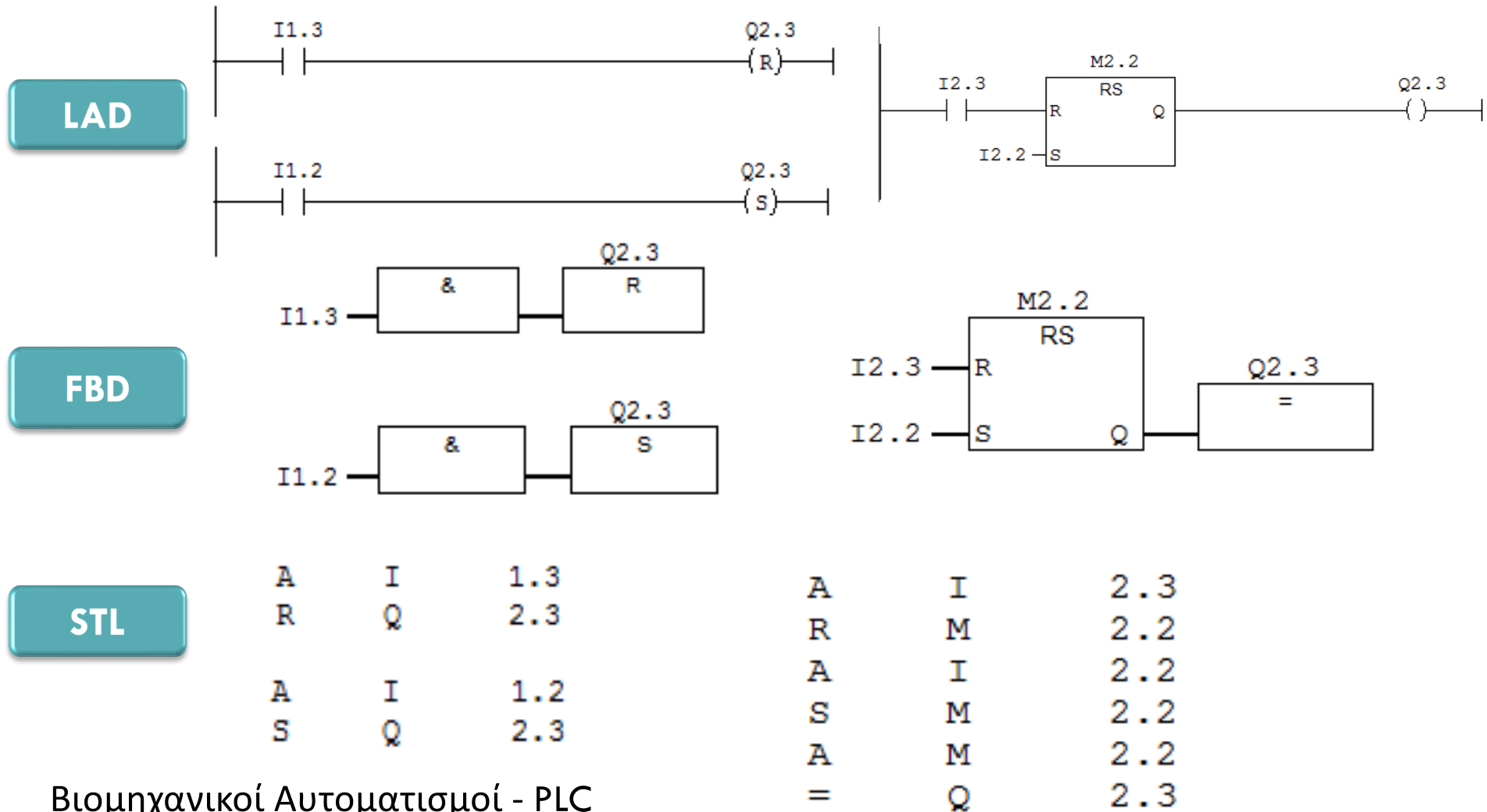
STL

A	I	1.2
A	I	2.2
=	Q	2.3

## ΛΟΓΙΚΗ ΕΝΤΟΛΗ : SET/RESET



## ΛΟΓΙΚΗ ΕΝΤΟΛΗ : RESET/SET





# ΠΑΝΕΠΙΣΤΗΜΙΟ ΔΥΤΙΚΗΣ ΑΤΤΙΚΗΣ

Σχολή Μηχανικών

Τμήμα Μηχανικών Βιομηχανικής Σχεδίασης και Παραγωγής

## ΠΑΡΑΔΕΙΓΜΑ

A I2.2  
= Q6.2

A Q6.2  
= Q6.4

A I4.4  
= Q6.2

I2.2	I4.4	Q6.2	Q6.4
0	0		
0	1		
1	0		
1	1		



# ΠΑΝΕΠΙΣΤΗΜΙΟ ΔΥΤΙΚΗΣ ΑΤΤΙΚΗΣ

Σχολή Μηχανικών

Τμήμα Μηχανικών Βιομηχανικής Σχεδίασης και Παραγωγής

## ΠΑΡΑΔΕΙΓΜΑ

NETWORK 1		NETWORK 2	
A	I1	AN	I3
A	M4.2	A	I4
=	M1.1	=	M1.3
A	I2	A	I1
AN	I3	A	I4
=	M1.2	=	M1.4
A	M1.1	AN	M1.3
ON	M1.2	O	M1.4
=	Q1.1	=	M4.2

		I1-I2	I1-I2	I1-I2	I1-I2
	a/a	00	01	10	11
I3-I4	00				
I3-I4	01				
I3-I4	10				
I3-I4	11				

Q1.1=;



# ΠΑΝΕΠΙΣΤΗΜΙΟ ΔΥΤΙΚΗΣ ΑΤΤΙΚΗΣ

Σχολή Μηχανικών

Τμήμα Μηχανικών Βιομηχανικής Σχεδίασης και Παραγωγής

## ΠΑΡΑΔΕΙΓΜΑ

### NETWORK 1

AN	I1
A	M4.2
=	M1.1
AN	I2
A	I3
=	M1.2
AN	M1.1
O	M1.2
=	Q1.1

### NETWORK 2

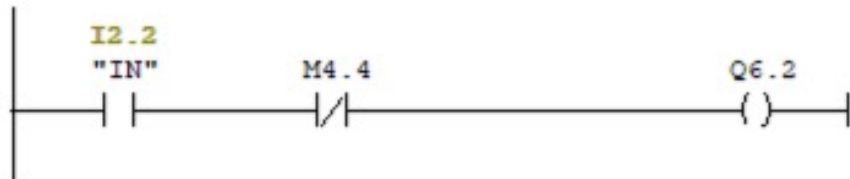
AN	I3
A	I4
=	M1.3
AN	I1
A	I4
=	M1.4
A	M1.3
ON	M1.4
=	M4.2

		I1-I2	I1-I2	I1-I2	I1-I2
	a/a	00	01	10	11
I3-I4	00				
I3-I4	01				
I3-I4	10				
I3-I4	11				

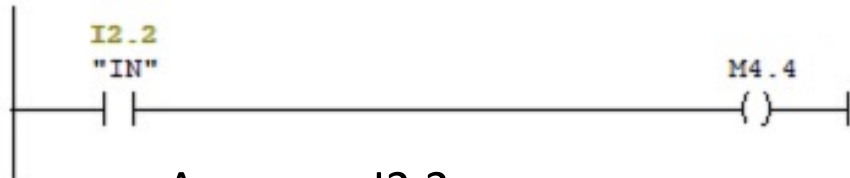
Q1.1=;



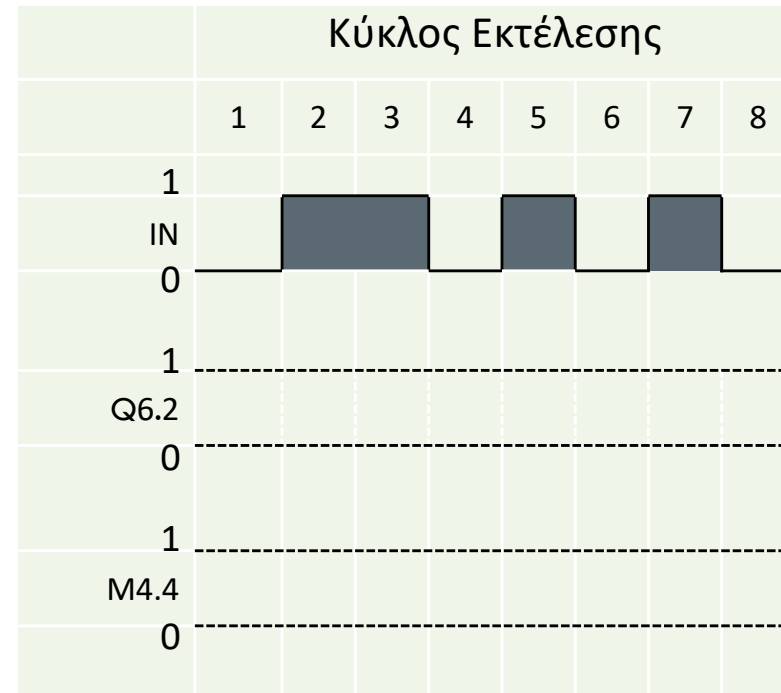
## ΠΑΡΑΔΕΙΓΜΑ



Network 2: Title:



A	I2.2
AN	M4.4
=	Q6.2
A	I2.2
=	M4.4

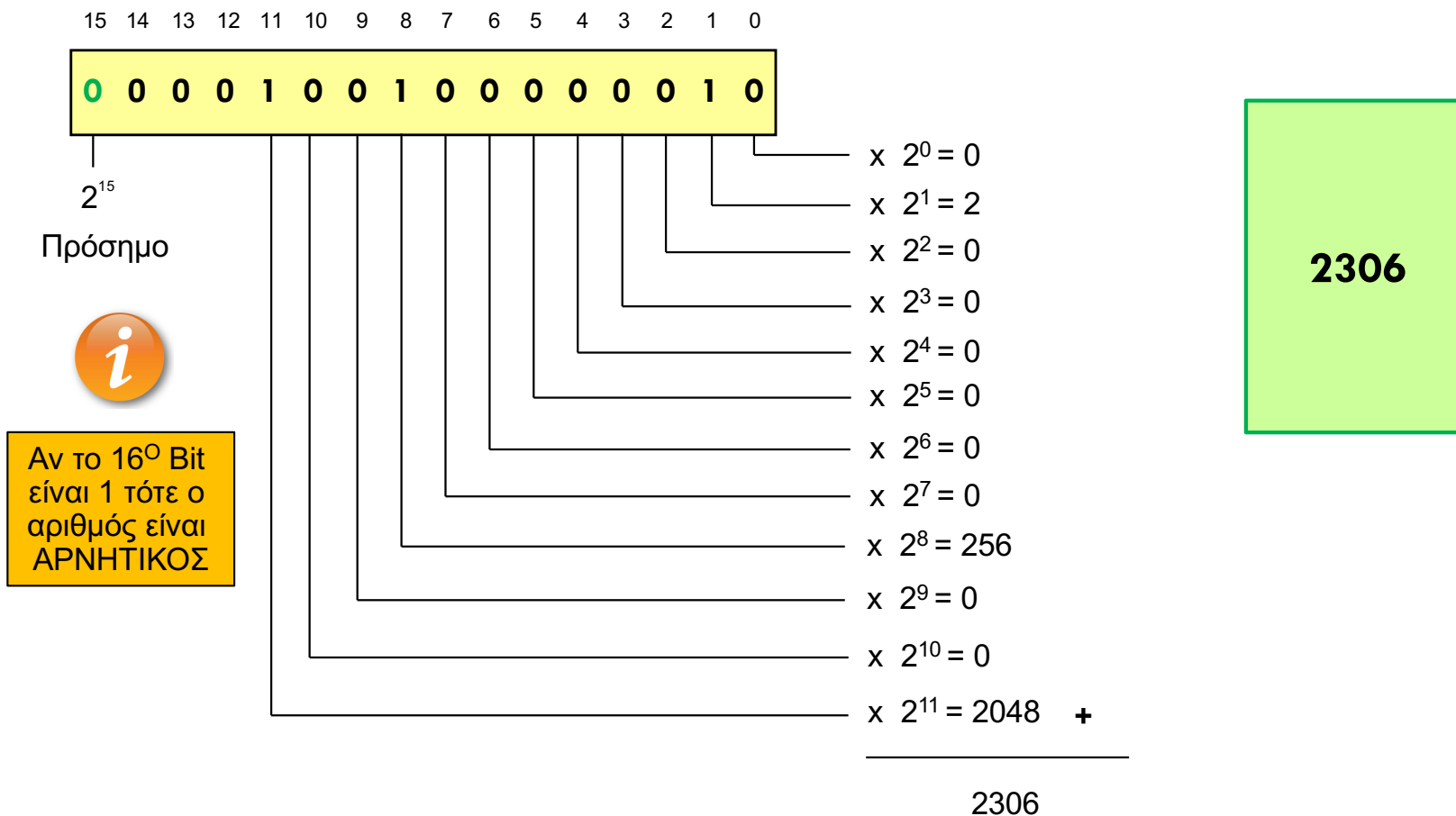




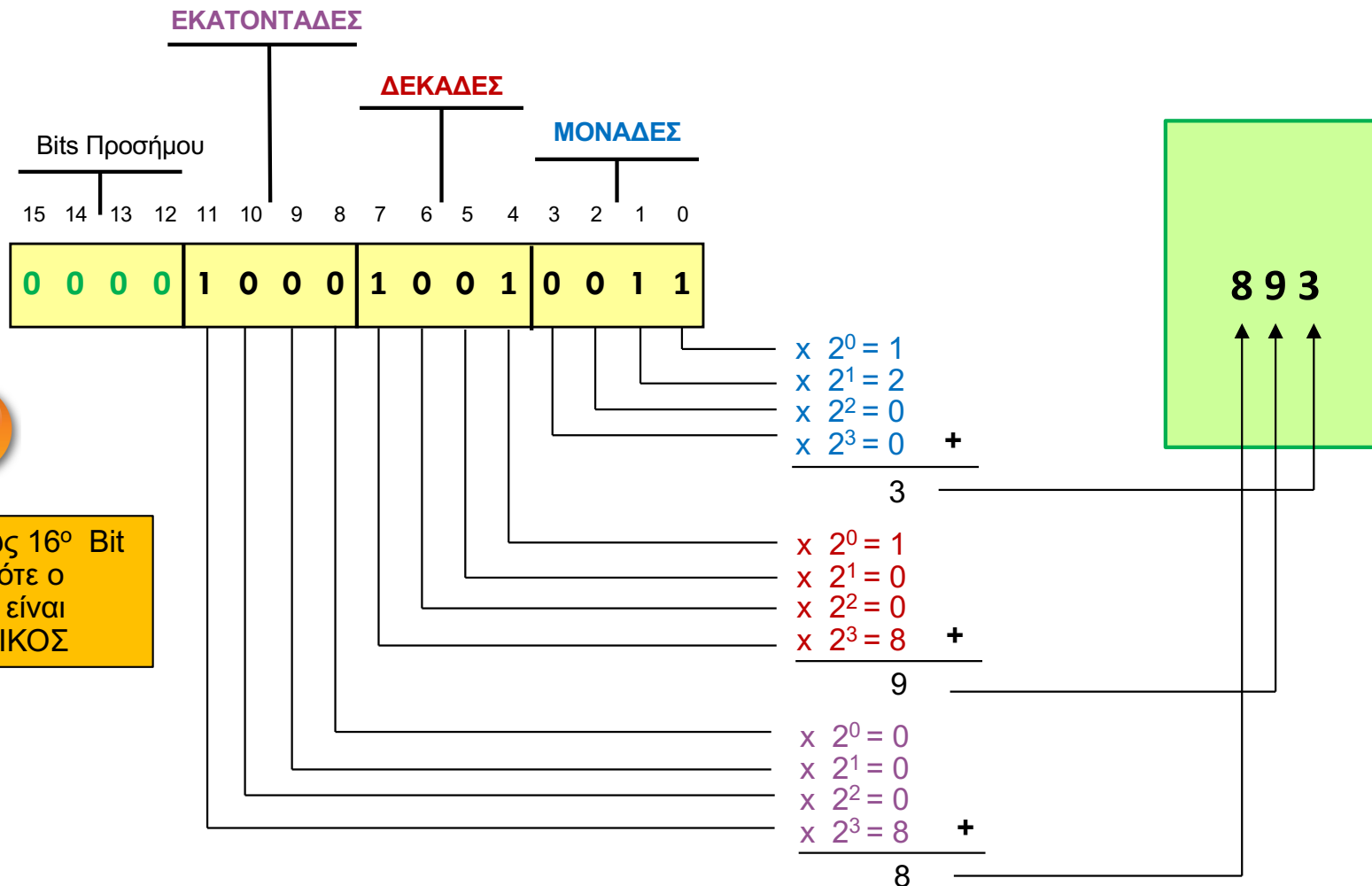
# Μεγέθη Δεδομένων

Address	BYTE							
	.7	.6	.5	.4	.3	.2	.1	.0
0	bit	bit	bit	bit	bit	bit	bit	bit
1	BYTE							
2	WORD							
3								
4	DOUBLE WORD							
5								
6								
7								
:								

## INTEGER – 16Bits

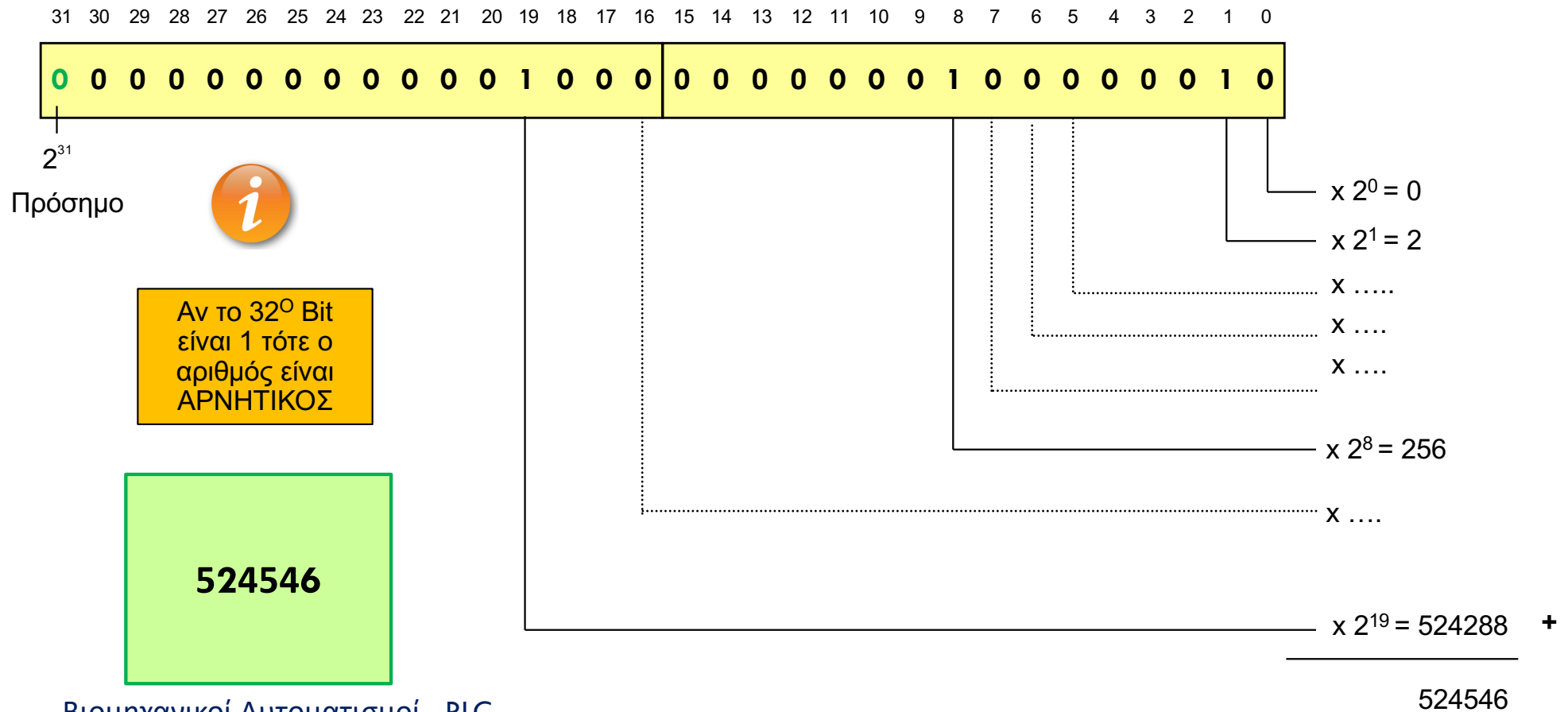


## BCD – 16Bits

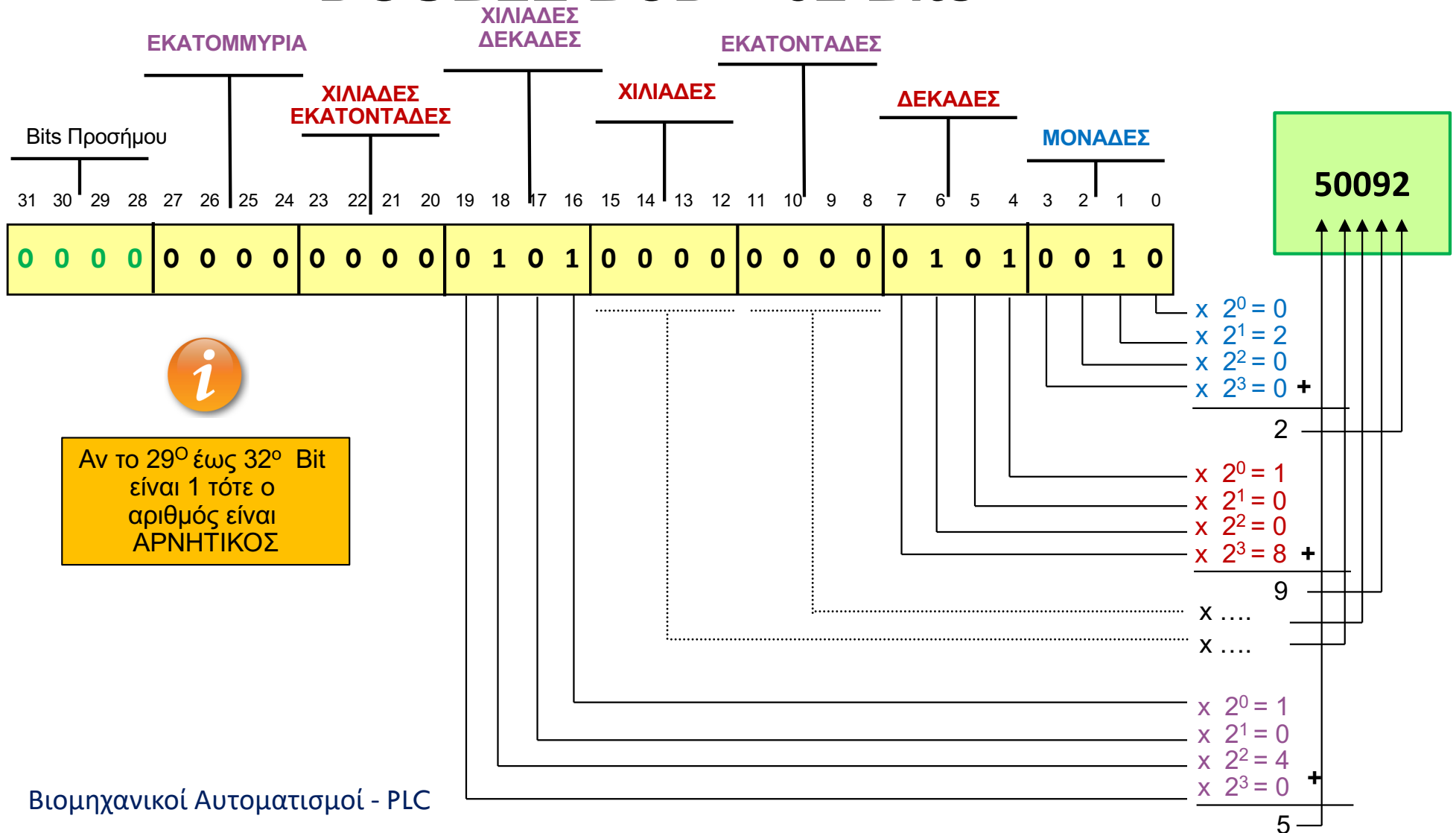


Αν το 13<sup>ο</sup> έως 16<sup>ο</sup> Bit είναι 1 τότε ο αριθμός είναι ΑΡΝΗΤΙΚΟΣ

## DOUBLE INTEGER – 32 Bits

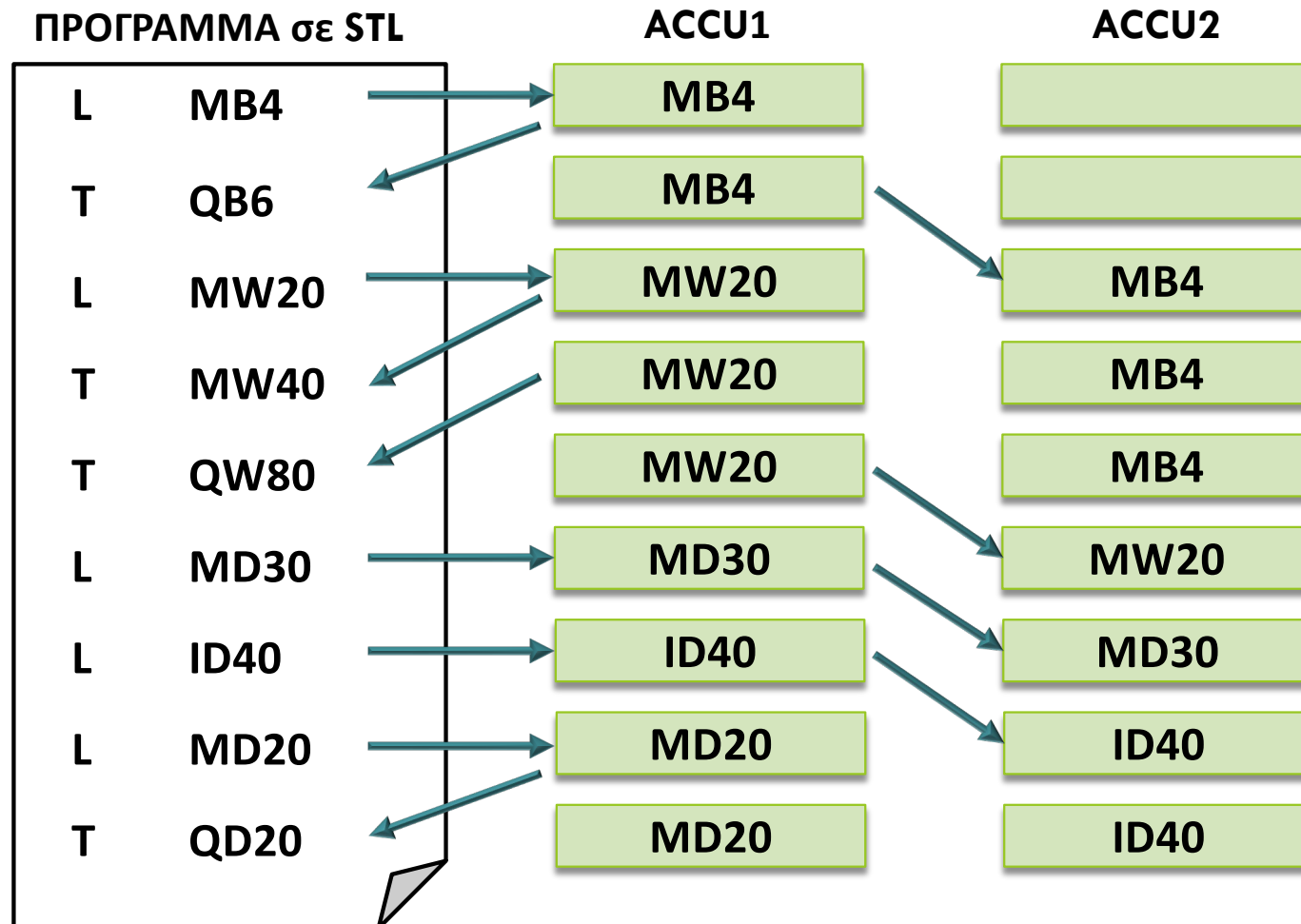


## DOUBLE BCD – 32 Bits



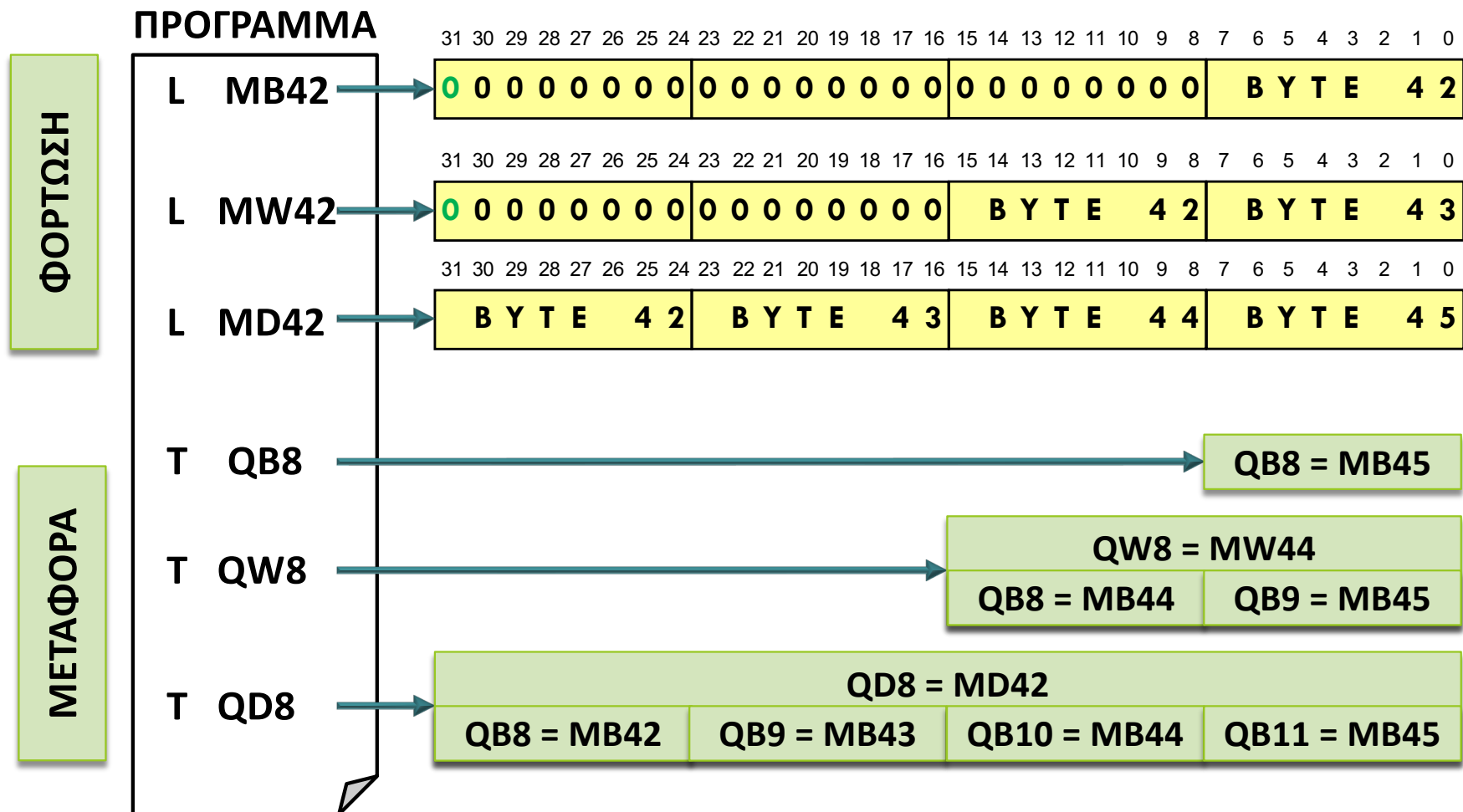


## ΦΟΡΤΩΣΗ ΚΑΙ ΜΕΤΑΦΟΡΑ





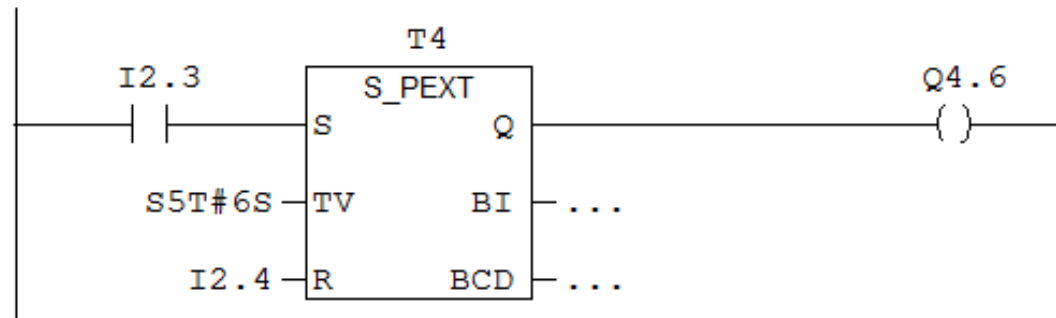
## ΦΟΡΤΩΣΗ ΚΑΙ ΜΕΤΑΦΟΡΑ



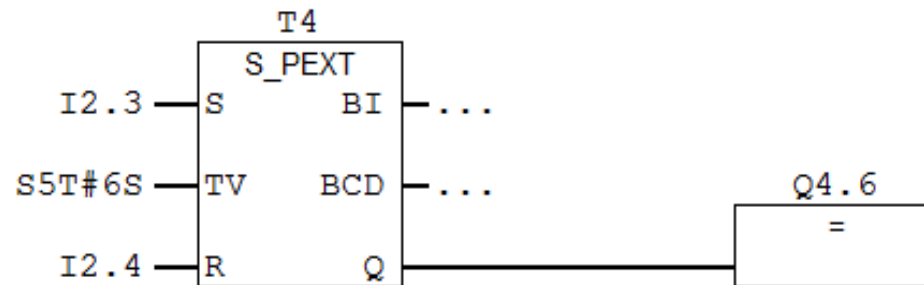


## TIMERS

LAD



FBD



STL

```

A      I      2.3
L      S5T#6S
SE     T      4
A      I      2.4
R      T      4
NOP    0
NOP    0
A      T      4
=      Q      4.6
    
```

## TIMERS

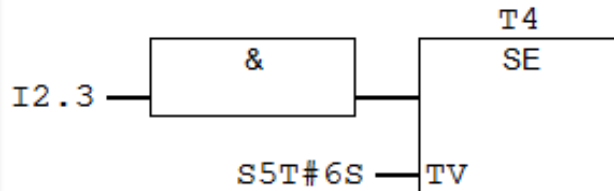
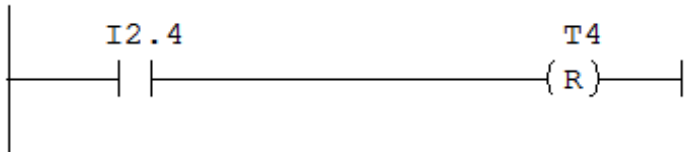
ΕΝΕΡΓΟΠΟΙΗΣΗ

LAD

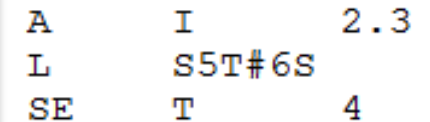


ΜΗΔΕΝΙΣΜΟΣ

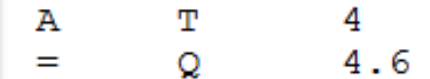
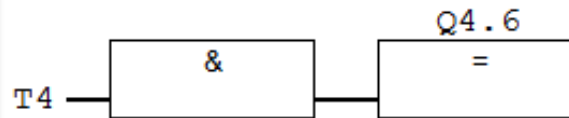
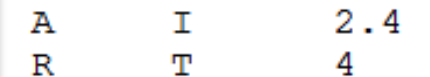
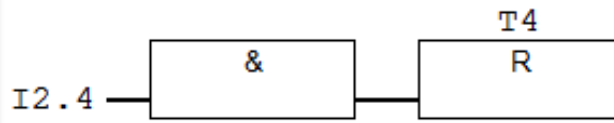
FBD



STL



ΕΡΩΤΗΣΗ



## ΠΡΟΓΡΑΜΜΑ

A	I	4.1
CU	C	2
A	I	1.5
CD	C	2
A	I	2.3
L	C#20	
S	C	2
A	I	5.7
R	C	2
L	C	2
T	MW	4
LC	C	2
T	QW	14
A	C	2
=	Q	1.3

## COUNTERS

**ΑΥΞΗΣΗ** της τιμής του **COUNTER**

**ΜΕΙΩΣΗ** της τιμής του **COUNTER**

**ΠΡΩΤΟΠΟΘΕΤΗΣΗ** τιμής στον **COUNTER**

**ΜΗΔΕΝΙΣΜΟΣ** του **COUNTER**

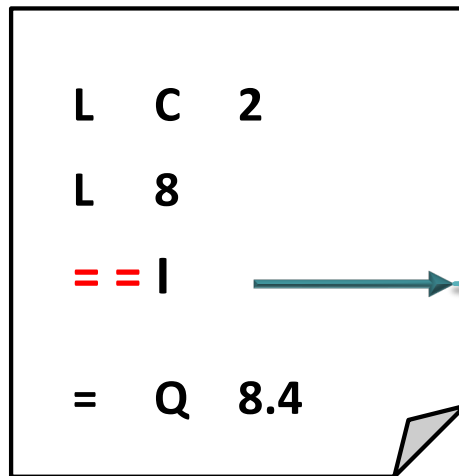
**ΔΙΑΒΑΣΜΑ** της τιμής του **COUNTER** σε **INTEGER FORMAT**

**ΔΙΑΒΑΣΜΑ** της τιμής του **COUNTER** σε **BCD FORMAT**

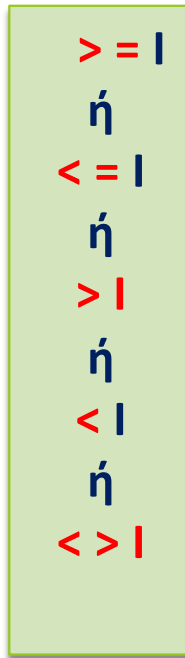
**ΔΙΑΒΑΣΜΑ** την **BIT** τιμή του **COUNTER**

## COUNTERS – ΣΥΓΚΡΙΣΗ

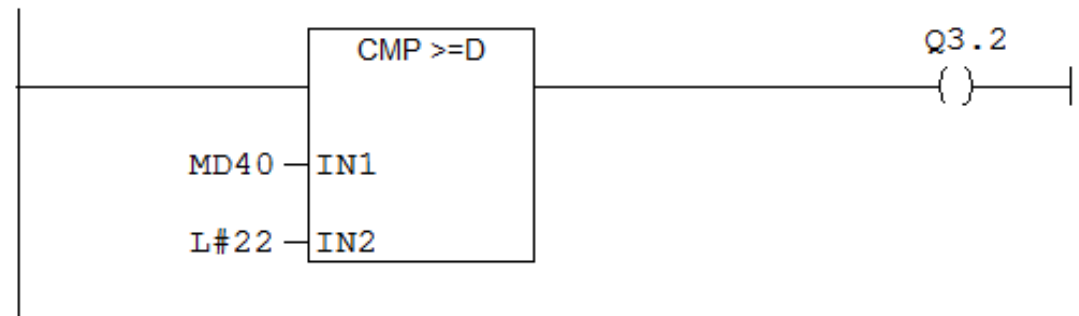
### ΣΥΓΚΡΙΣΗ ΜΕ INTEGER



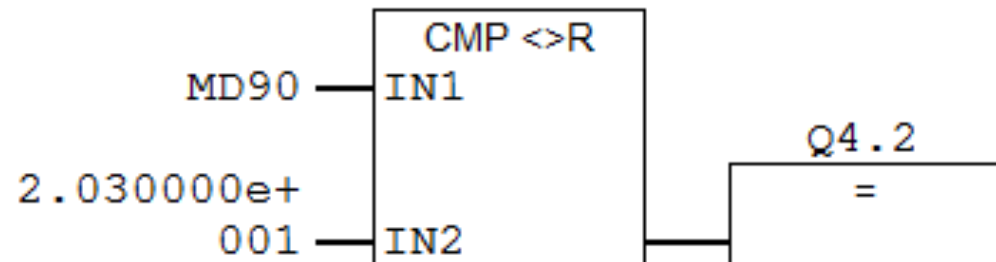
Έξοδος 0 για ΌΧΙ  
Έξοδος 1 για ΝΑΙ



### ΣΥΓΚΡΙΣΗ ΜΕ DOUBLE INTEGER

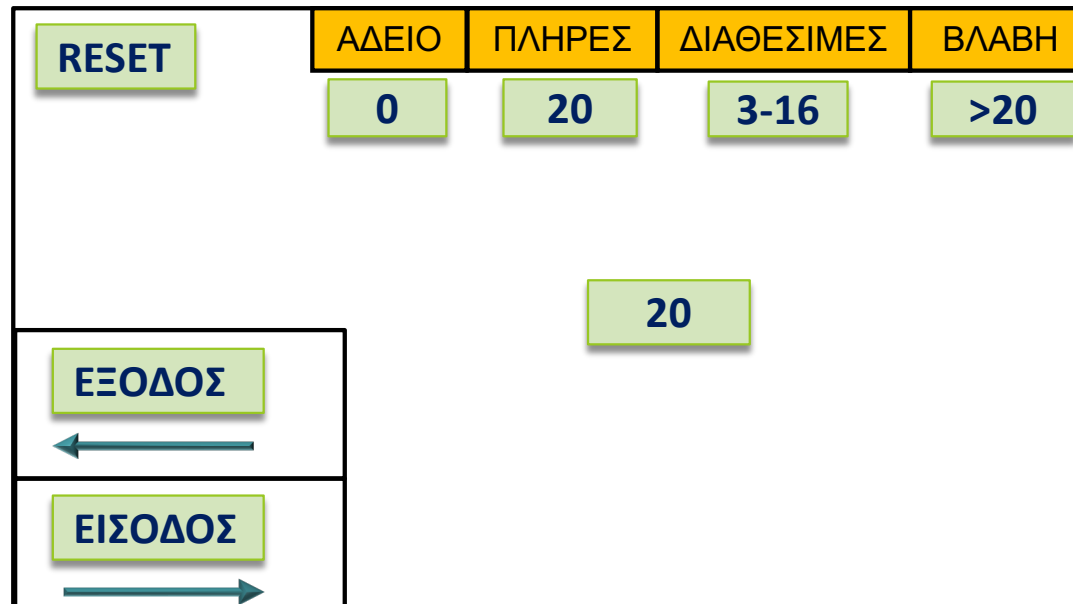


### ΣΥΓΚΡΙΣΗ ΜΕ REAL



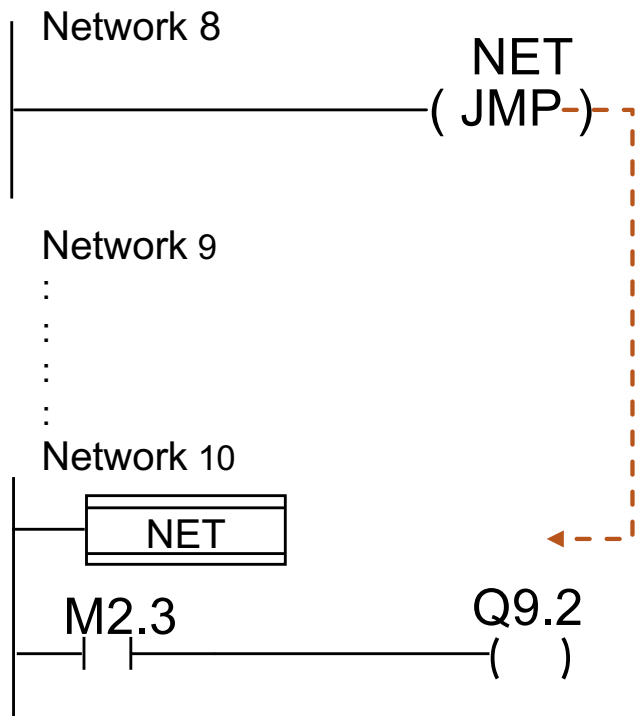
# ΠΑΡΑΔΕΙΓΜΑ ΜΕ COUNTERS

## Χώρος Στάθμευσης Αυτοκινήτων

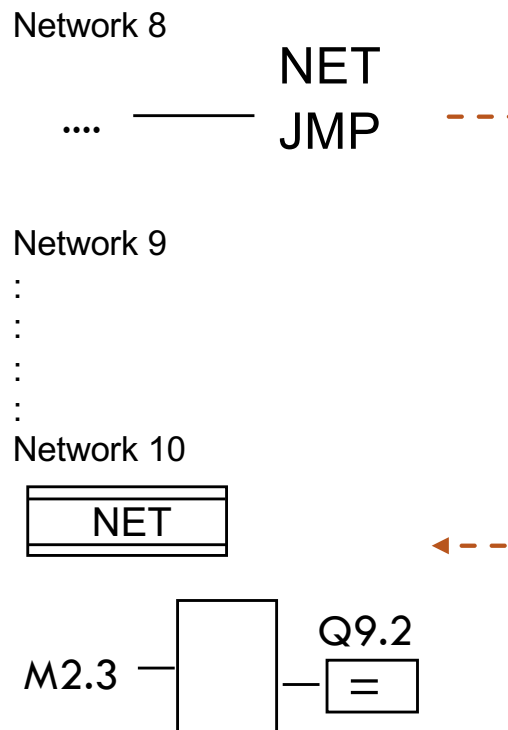


# Εντολές Μεταπήδησης

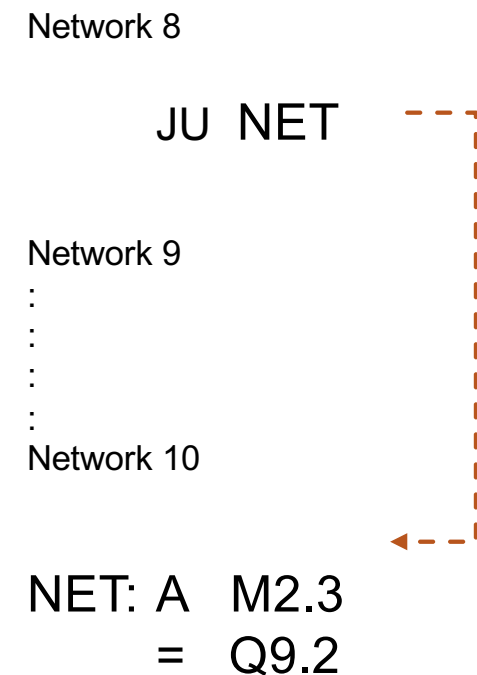
LAD



FBD



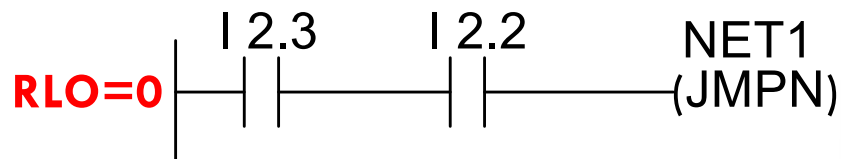
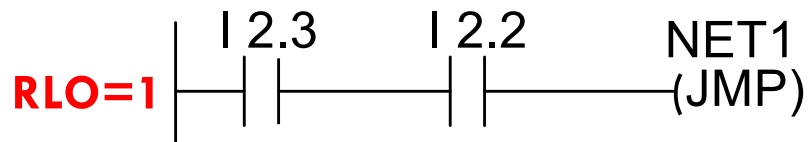
STL



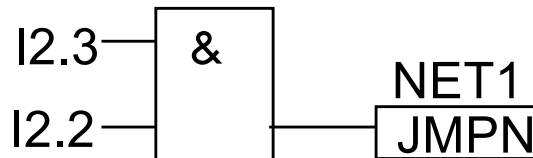
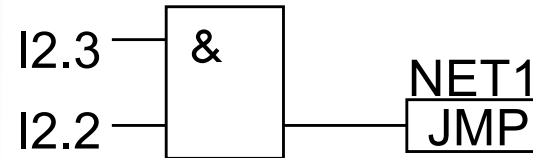


## Εντολές Μεταπήδησης

LAD



FBD

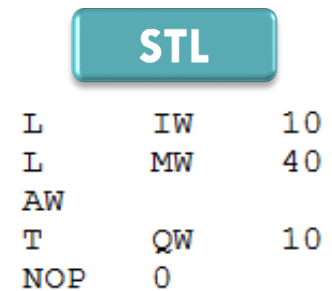
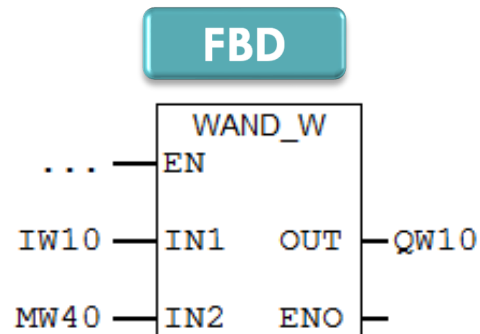
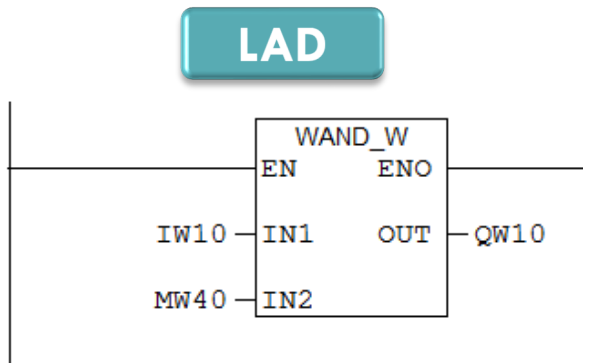


STL

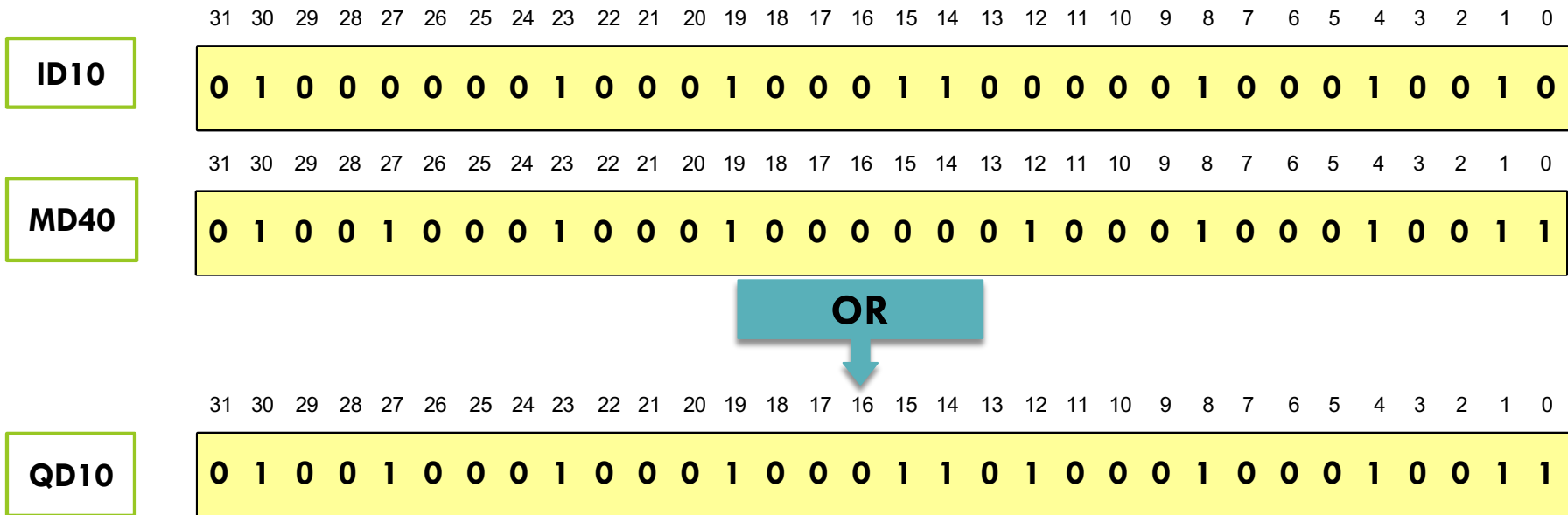
A I2.3  
A I2.2  
JC NET1

A I2.3  
A I2.2  
JCN NET1

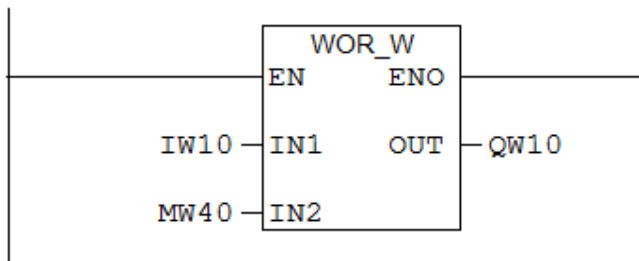
## ΠΡΑΞΕΙΣ ΨΗΦΙΑΚΗΣ ΛΟΓΙΚΗΣ - AND



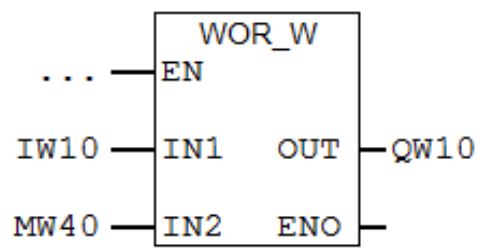
## ΠΡΑΞΕΙΣ ΨΗΦΙΑΚΗΣ ΛΟΓΙΚΗΣ - OR



**LAD**



**FBD**



**STL**

```

L    IW    10
L    MW    40
OW
T    QW    10
NOP    0
    
```

## ΠΡΑΞΕΙΣ ΨΗΦΙΑΚΗΣ ΛΟΓΙΚΗΣ - XOR

**ID10**

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0  
 0 1 0 0 0 0 0 0 1 0 0 0 1 0 0 0 1 1 0 0 0 0 0 1 0 0 0 1 0 0 1 0

**MD40**

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0  
 0 1 0 0 1 0 0 0 1 0 0 0 1 0 0 0 0 0 0 1 0 0 0 1 0 0 0 1 0 0 1 1

**XOR**

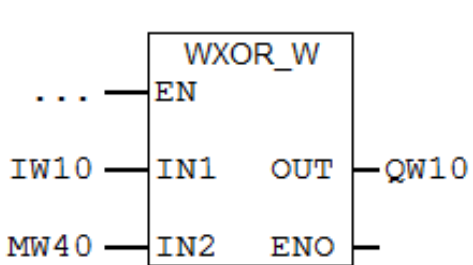
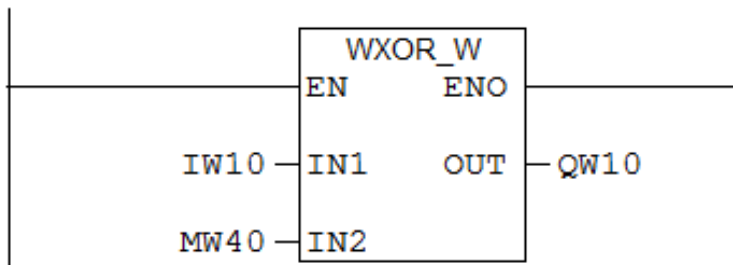
**QD10**

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0  
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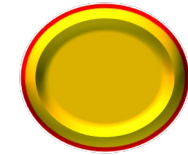
**LAD**

**FBD**

**STL**



```
L    IW    10
L    MW    40
XOW
T    QW    10
NOP    0
```



## ΠΑΡΑΔΕΙΓΜΑ

