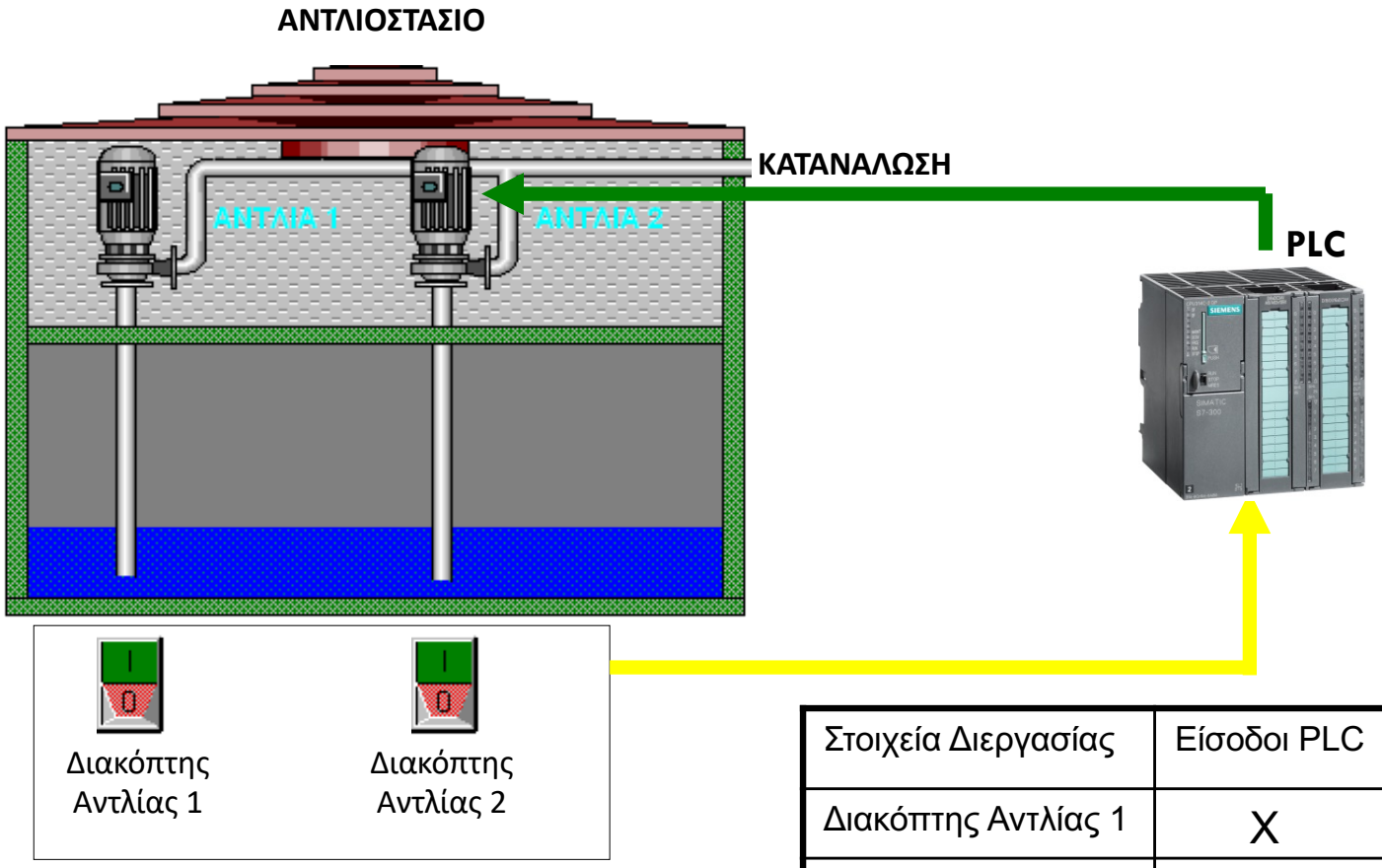
ΠΑΝΕΠΙΣΤΗΜΙΟ ΔΥΤΙΚΗΣ ΑΤΤΙΚΗΣ

Σχολή Μηχανικών
Τμήμα Μηχανικών Βιομηχανικής Σχεδίασης και Παραγωγής

Βιομηχανικοί Αυτοματισμοί - PLC

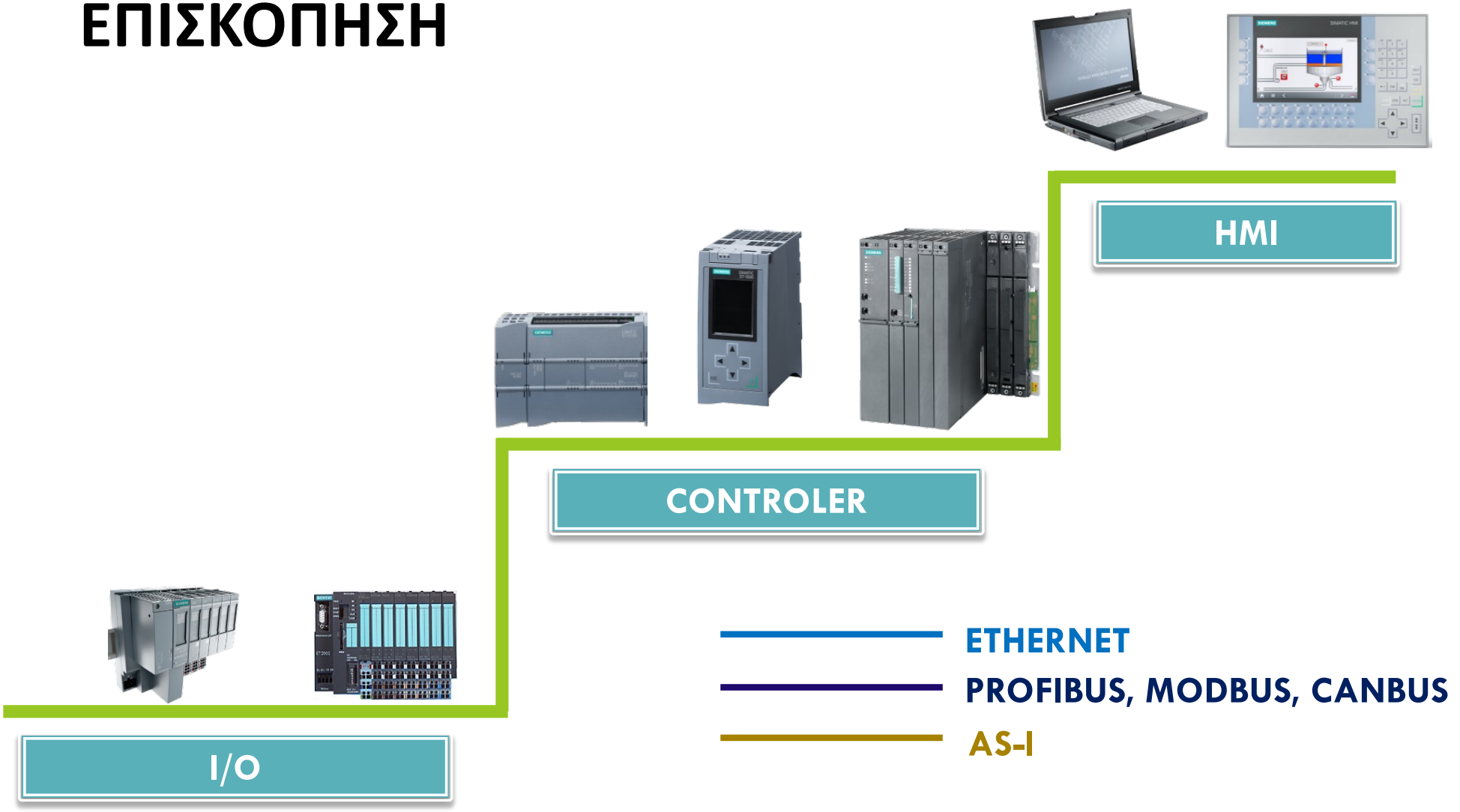
Θεοχάρης Ευστάθιος

ΔΙΕΡΓΑΣΙΑ

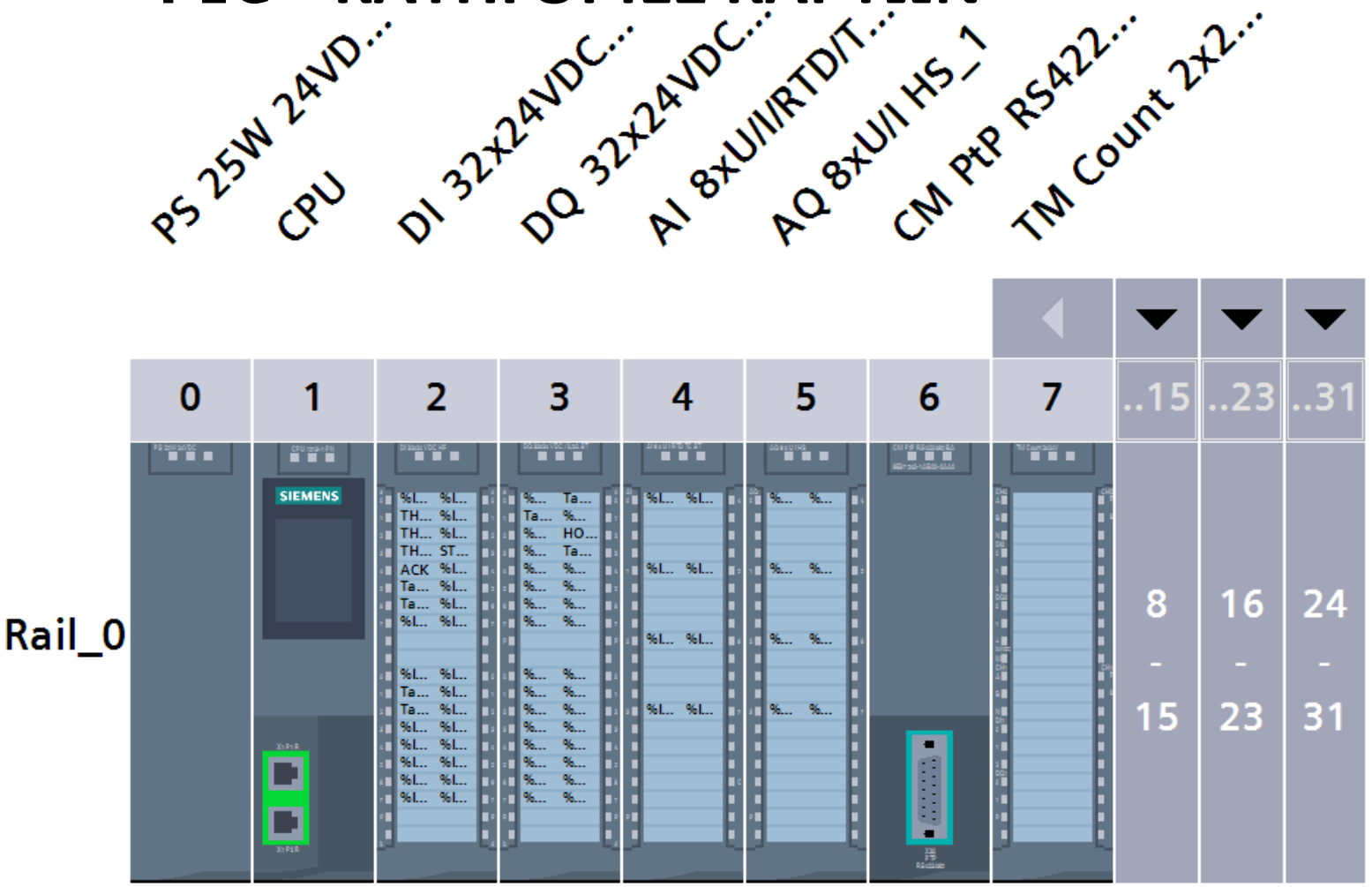


Στοιχεία Διεργασίας	Είσοδοι PLC	Έξοδοι PLC
Διακόπτης Αντλίας 1	X	
Διακόπτης Αντλίας 2	X	
Αντλία 1		X
Αντλία 2		X

ΕΠΙΣΚΟΠΗΣΗ



PLC - ΚΑΤΗΓΟΡΙΕΣ ΚΑΡΤΩΝ

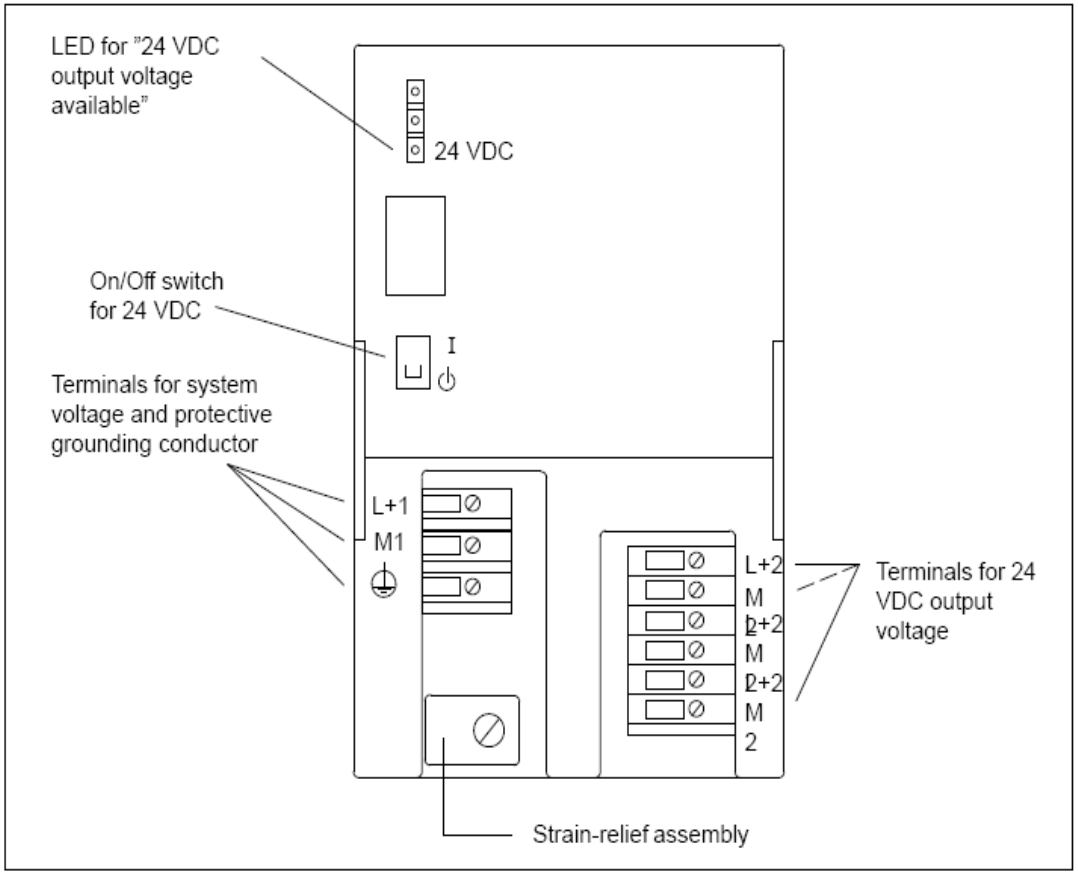


PLC - ΚΑΤΗΓΟΡΙΕΣ ΚΑΡΤΩΝ

- **RACK** : Ράγα στήριξης
- **PS** (Power Supply) : Τροφοδοτικό
- **CPU** : Κεντρική Μονάδα (επεξεργαστής)
- **SM** (Signal Module) : Κάρτα Σημάτων
  - Εισόδων : Ψηφιακών, Αναλογικών
  - Εξόδων : Ψηφιακών, Αναλογικών
- **CM** (ή **CP**) : Κάρτα Επικοινωνίας
- **TM** (ή **FM**) : Κάρτα για PID, Positioning, CAM, Counting, κλπ

ΤΡΟΦΟΔΟΤΙΚΟ

Wiring schematic of the PS 305; 2 A



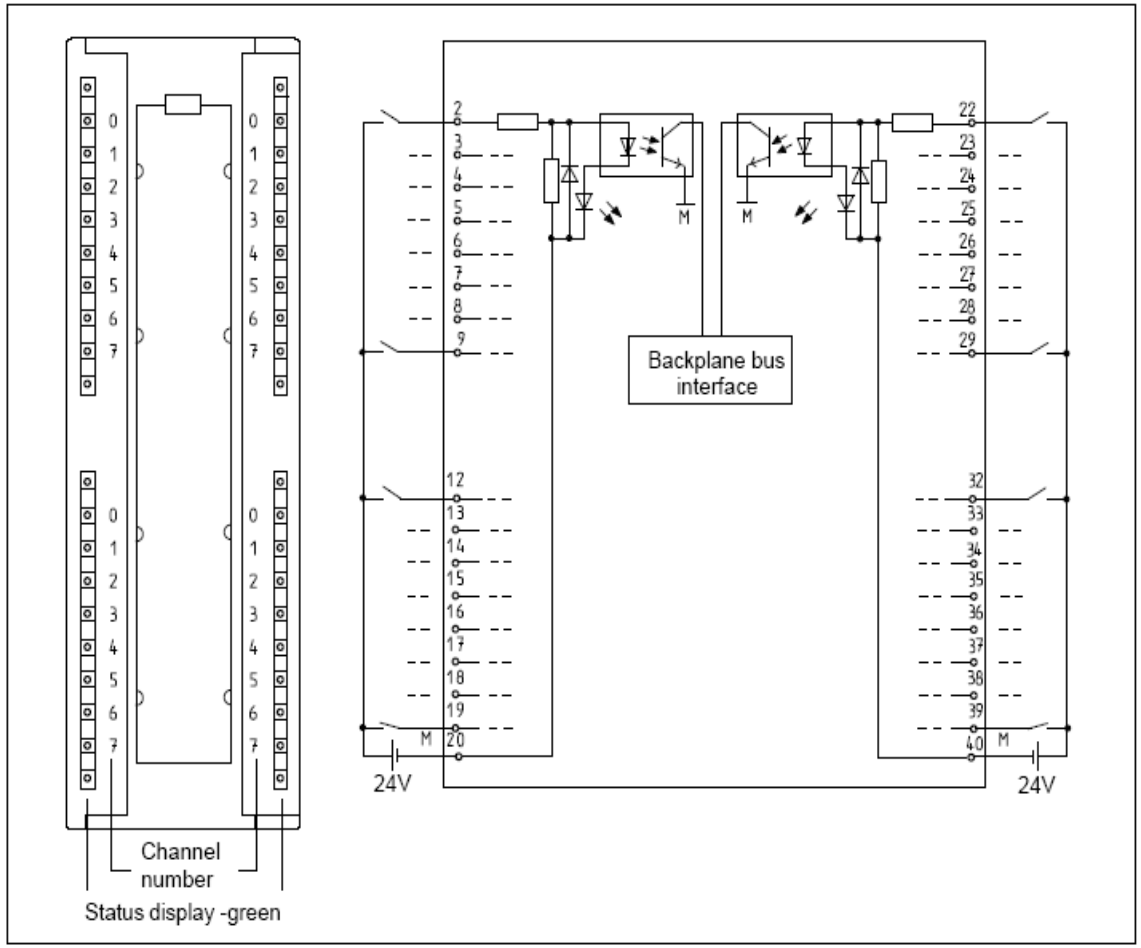
Wiring Schematic of the PS 305 Power Supply Module (2 A)

CPU


CPU315-2 DP
SF
BF
SIEMENS
MAINT
DC5V
FRCE
RUN
STOP
PUSH
RUN
STOP
MRES
SIMATIC
S7-300
2

DI – ΨΗΦΙΑΚΟΙ ΕΙΣΟΔΟΙ

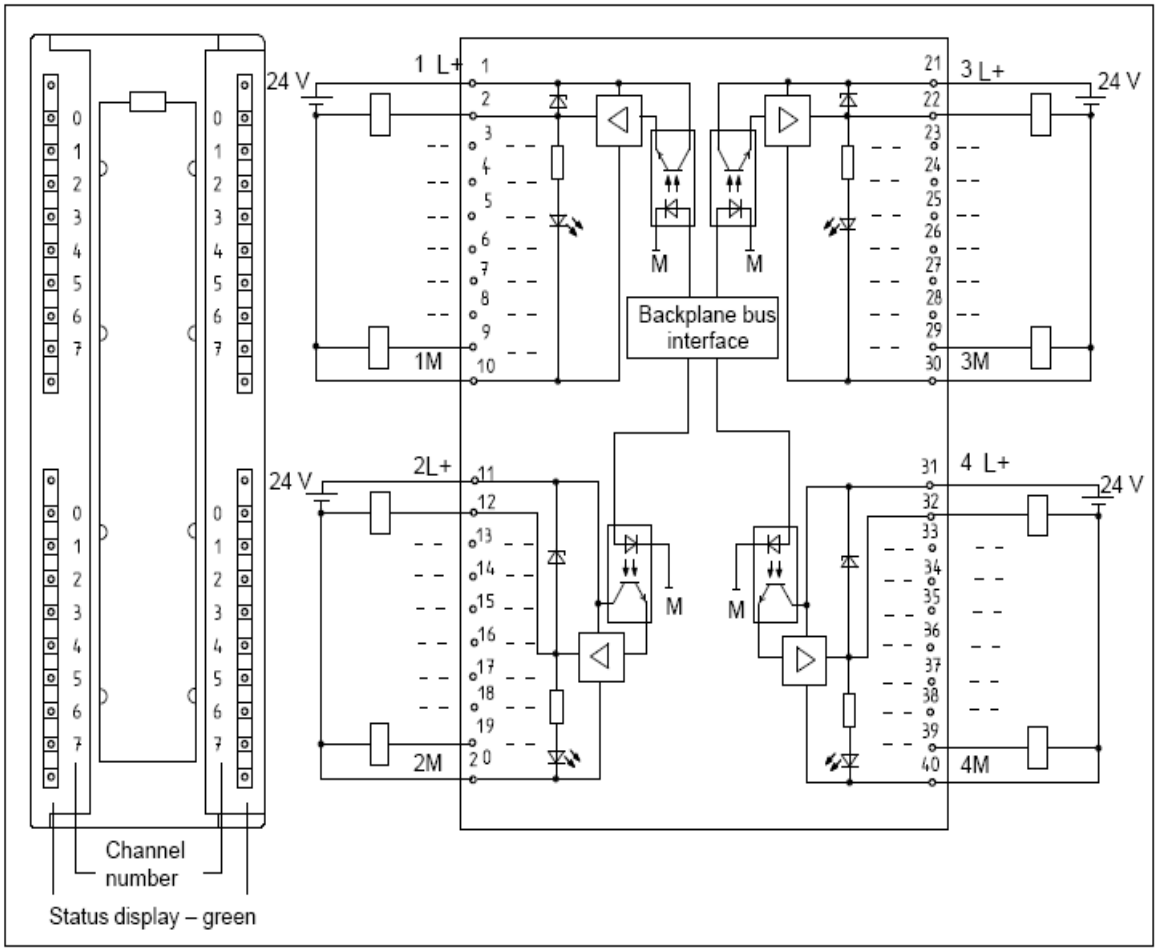
Terminal assignment and block diagram of the SM 321; DI 32 × 24 VDC



Module View and Block Diagram of the Digital Input Module SM 321; DI 32×24 VDC

DO – ΨΗΦΙΑΚΕΣ ΕΞΟΔΟΙ

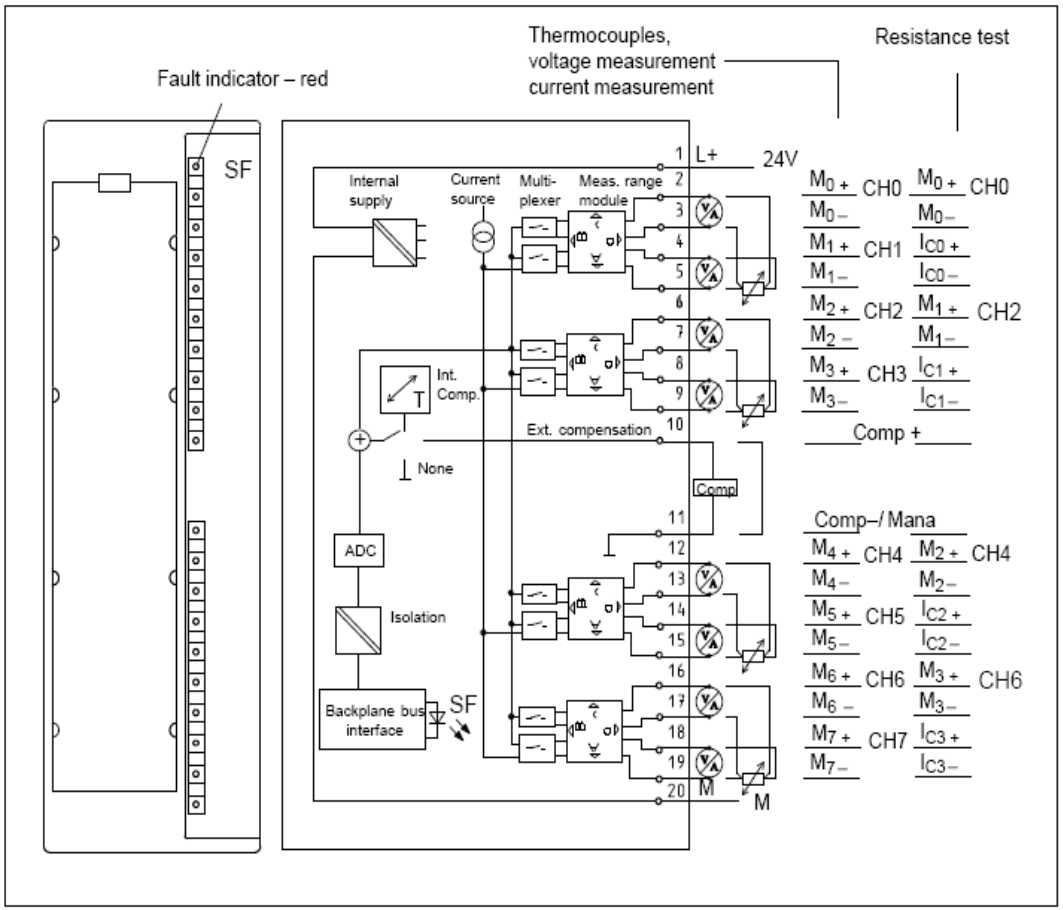
Module View and Block Diagram of the SM 322; DO 32 × 24 VDC/ 0.5 A



Module View and Block Diagram of Digital Output Module SM 322; DO 32 × 24 VDC/0.5 A

AI – ΑΝΑΛΟΓΙΚΕΣ ΕΙΣΟΔΟΙ

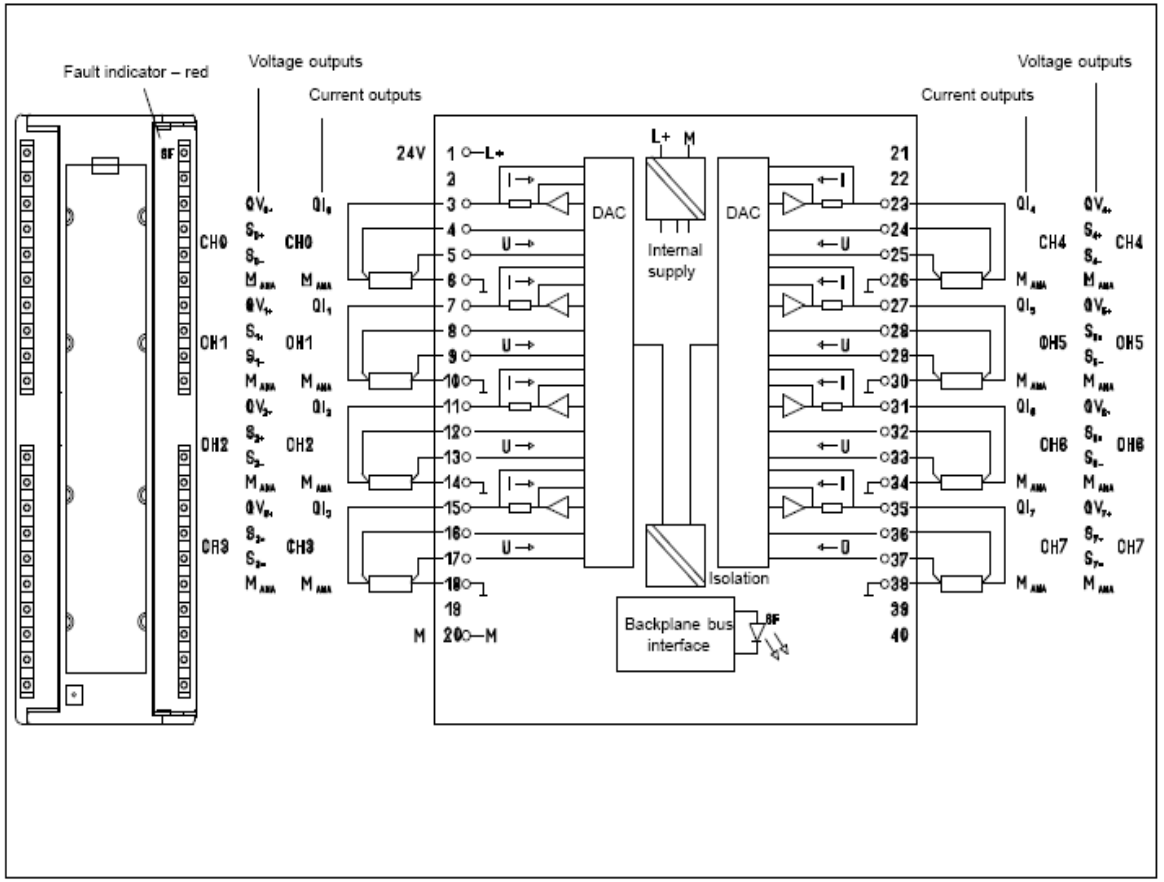
Terminal connection diagram and block diagram of the SM 331; AI 8 × 12 bits



Module View and Block Diagram of the Analog Input Module SM 331; AI 8 × 12 bits

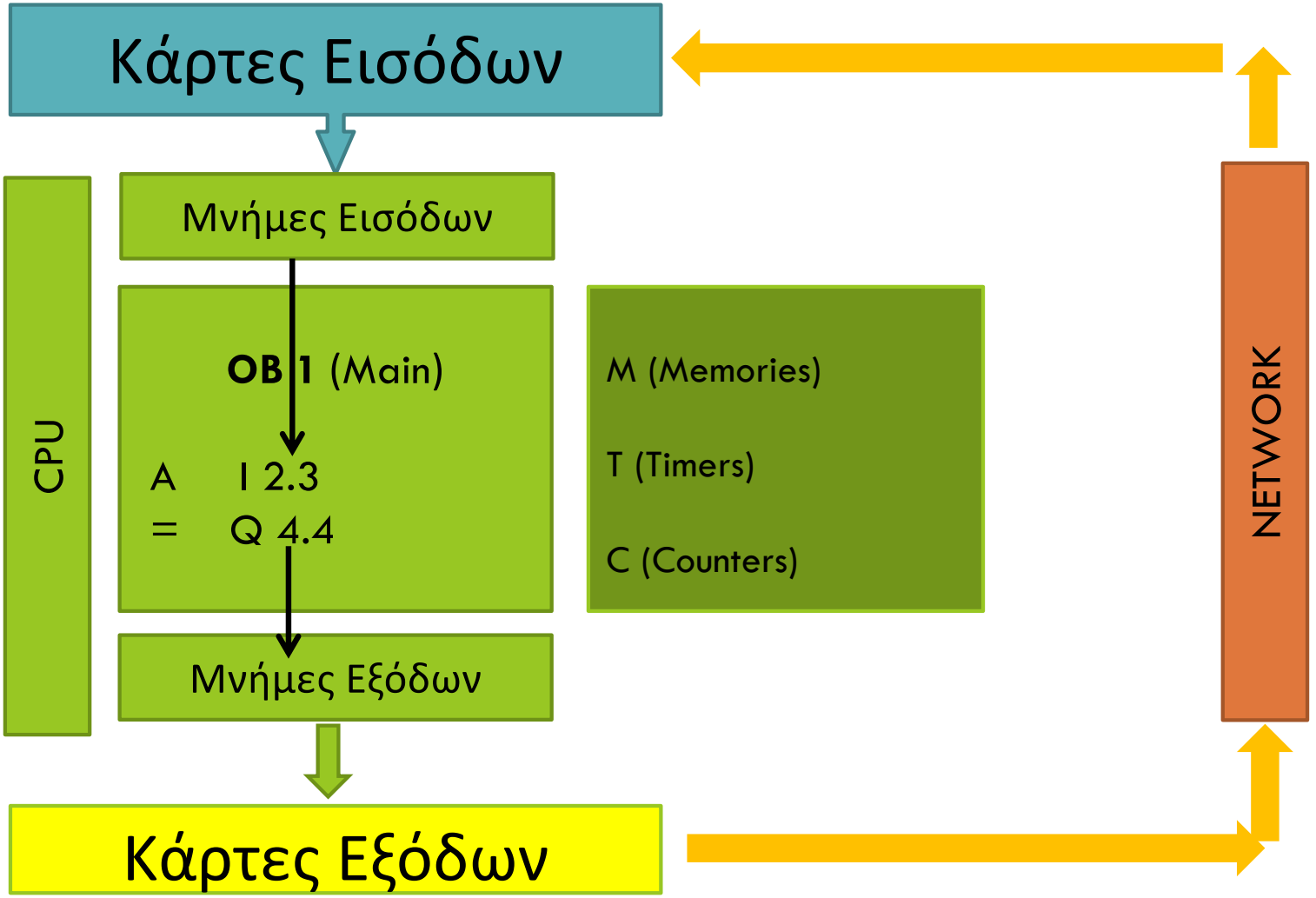
ΑΟ – ΑΝΑΛΟΓΙΚΕΣ ΕΞΟΔΟΙ

Terminal connection and block diagram of analog output module SM 332; AO 8 × 12 bits

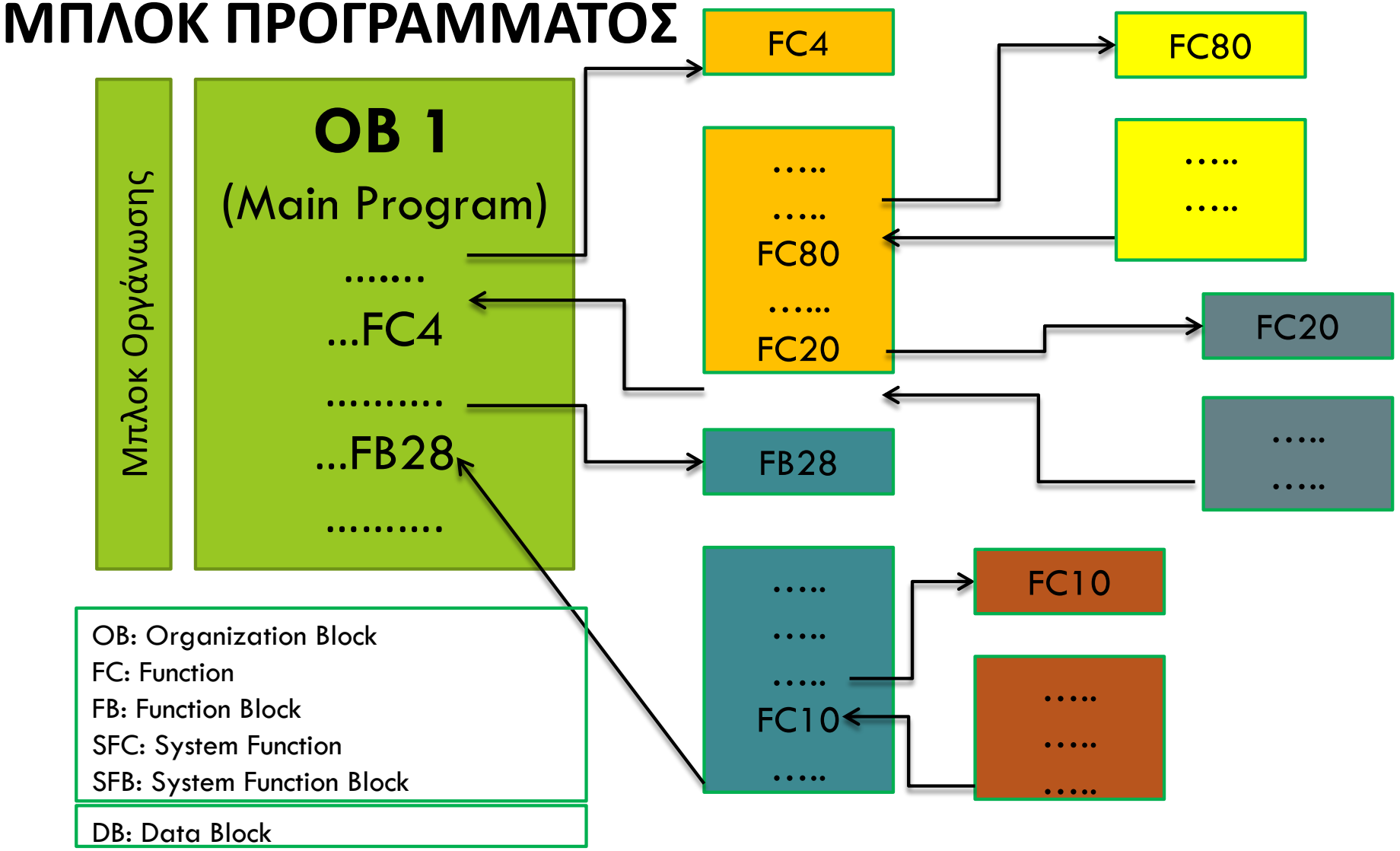


Module View and Block Diagram of the Analog Output Module SM 332; AO 8 × 12 bits

ΚΥΚΛΙΚΗ ΕΠΕΞΕΡΓΑΣΙΑ (ΚΥΚΛΟΣ ΠΡΟΓΡΑΜΜΑΤΟΣ P L C)



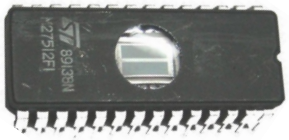
ΜΠΛΟΚ ΠΡΟΓΡΑΜΜΑΤΟΣ

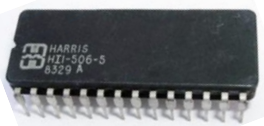


PLC MEMORIES

LOAD MEMORY	WORK MEMORY	RETAIN MEMORY
RAM EPROM EEPROM	RAM	EEPROM

RAM 

EPROM 

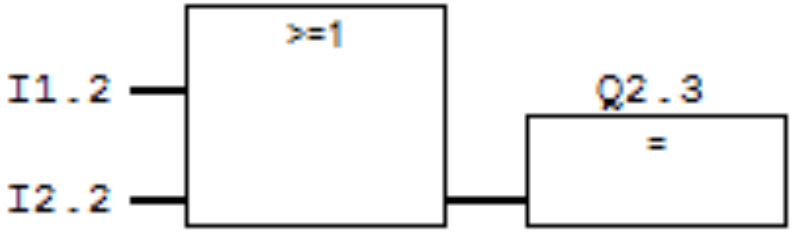
EEPROM 

ΛΟΓΙΚΗ ΕΝΤΟΛΗ : OR

ΛΟΓΙΚΟΣ ΠΙΝΑΚΑΣ		
I1.2	I2.2	Q2.3
0	0	0
0	1	1
1	0	1
1	1	1

LAD

FBD



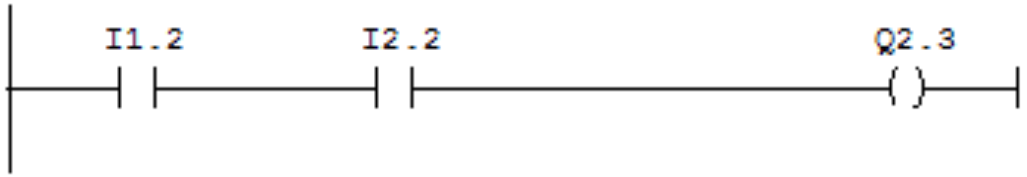
STL

```
O       I       1.2
O       I       2.2
=       Q       2.3
```

ΛΟΓΙΚΗ ΕΝΤΟΛΗ : AND

ΛΟΓΙΚΟΣ ΠΙΝΑΚΑΣ		
I1.2	I2.2	Q2.3
0	0	0
0	1	0
1	0	0
1	1	1

LAD



FBD

STL

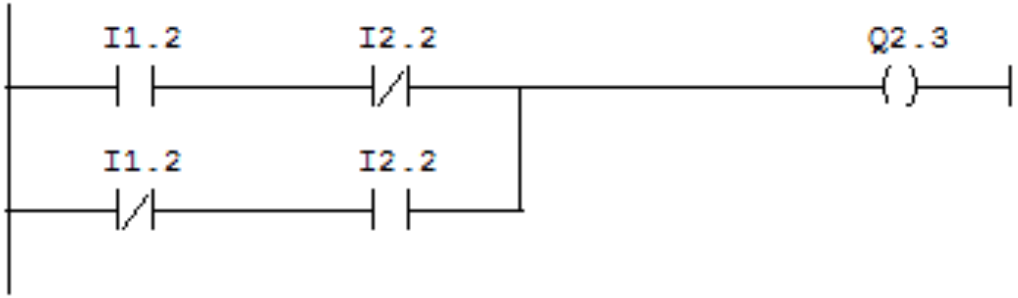
```
A     I     1.2
A     I     2.2
=     Q     2.3
```

ΛΟΓΙΚΗ ΕΝΤΟΛΗ : XOR

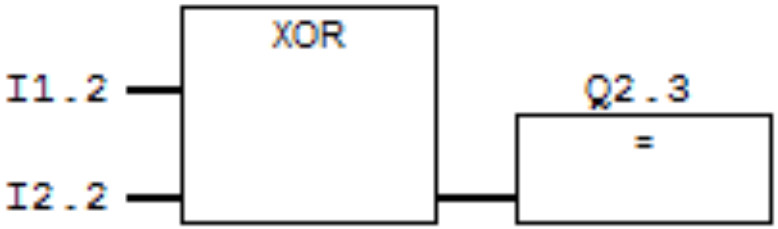
(Exclusive OR)

ΛΟΓΙΚΟΣ ΠΙΝΑΚΑΣ		
I1.2	I2.2	Q2.3
0	0	0
0	1	1
1	0	1
1	1	0

LAD



FBD



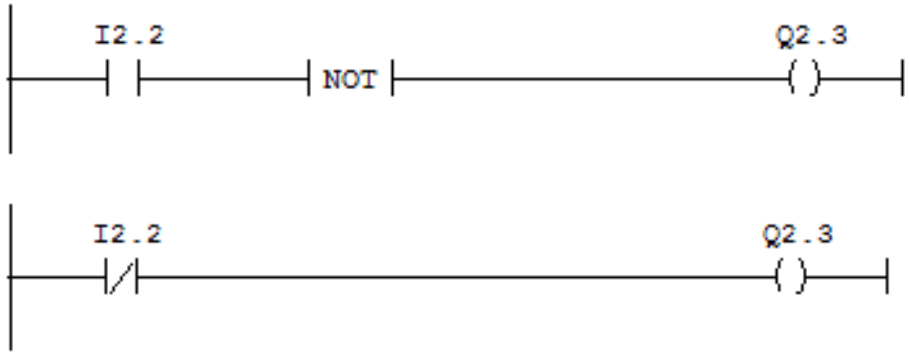
STL

```
X    I    1.2
X    I    2.2
=    Q    2.3
```

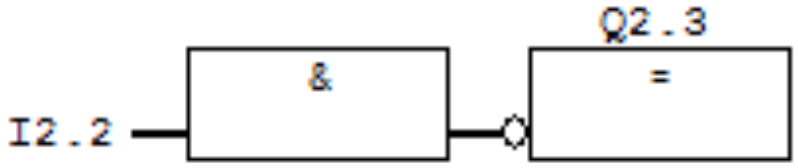
ΛΟΓΙΚΗ ΕΝΤΟΛΗ : NOT

ΛΟΓΙΚΟΣ ΠΙΝΑΚΑΣ	
I2.2	Q2.3
1	0
0	1

LAD



FBD



STL

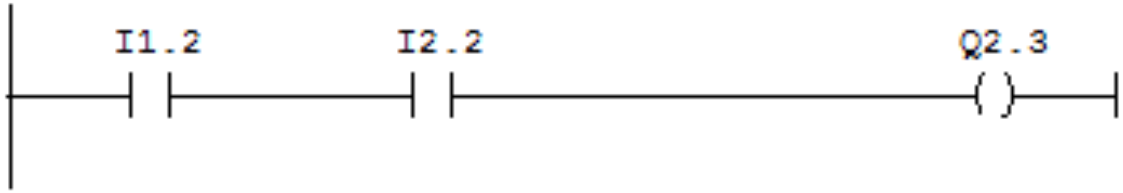
```
AN      I       2.2
=       Q       2.3

A       I       2.2
NOT
=       Q       2.3
```

ΛΟΓΙΚΗ ΕΝΤΟΛΗ : =

(Assignment)

LAD



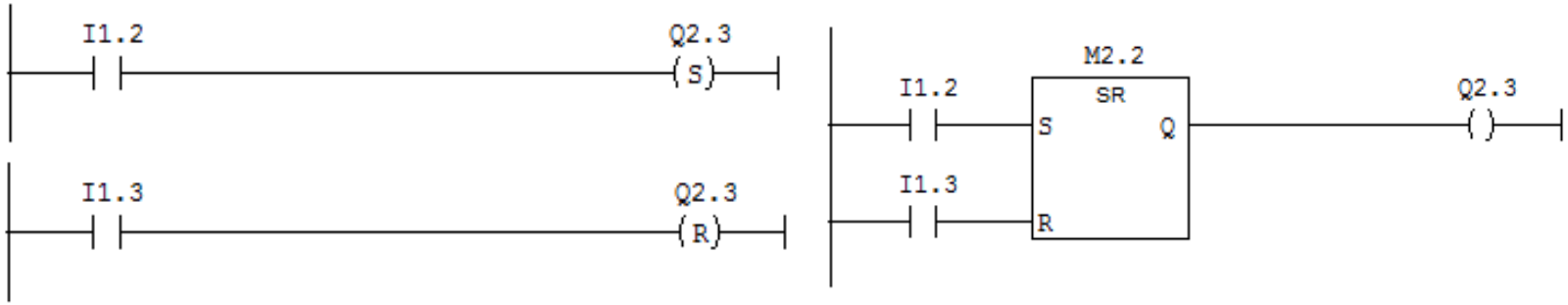
FBD

STL

```
A     I     1.2
A     I     2.2
=     Q     2.3
```

ΛΟΓΙΚΗ ΕΝΤΟΛΗ : SET/RESET

LAD



FBD

STL

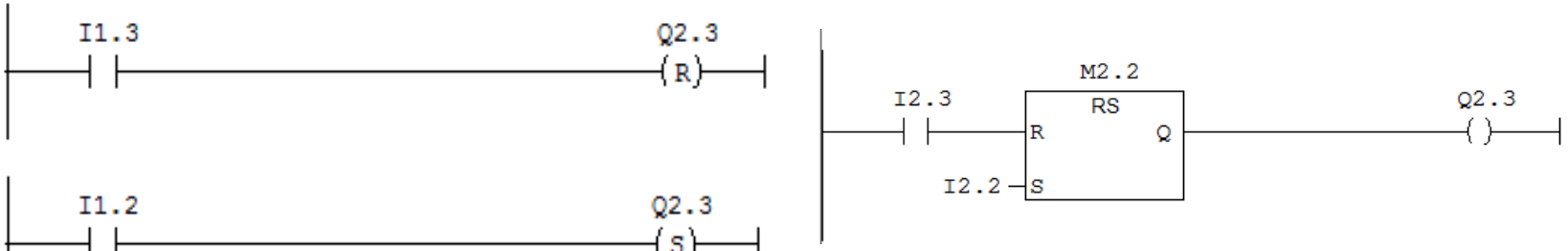
```
A     I     1.2
S     Q     2.3

A     I     1.3
R     Q     2.3
```

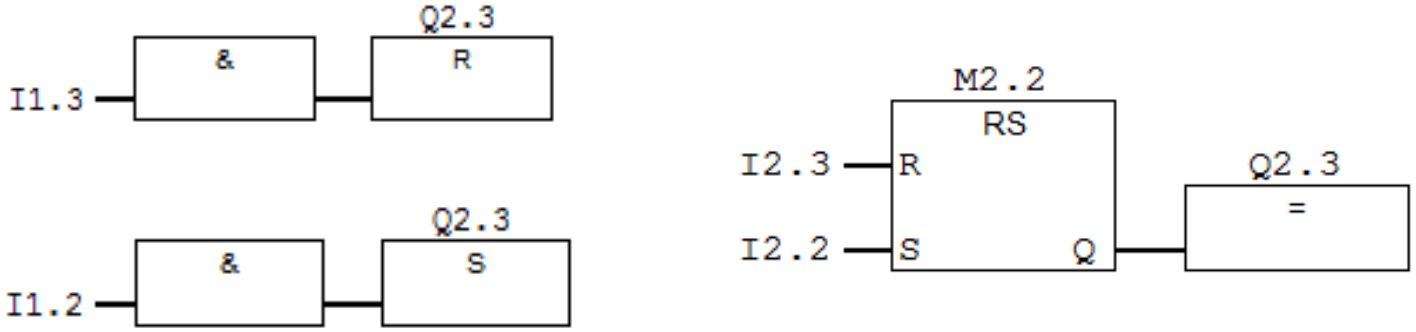
```
A     I     1.2
S     M     2.2
A     I     1.3
R     M     2.2
A     M     2.2
=     Q     2.3
```

ΛΟΓΙΚΗ ΕΝΤΟΛΗ : RESET/SET

LAD



FBD



STL

```
A     I     1.3
R     Q     2.3

A     I     1.2
S     Q     2.3
```

```
A     I     2.3
R     M     2.2
A     I     2.2
S     M     2.2
A     M     2.2
=     Q     2.3
```

ΠΑΡΑΔΕΙΓΜΑ

```
A    I2.2
=    Q6.2

A    Q6.2
=    Q6.4

A    I4.4
=    Q6.2
```

I2.2	I4.4	Q6.2	Q6.4
0	0		
0	1		
1	0		
1	1		

ΠΑΡΑΔΕΙΓΜΑ

NETWORK 1	
A	I1
A	M4.2
=	M1.1
A	I2
AN	I3
=	M1.2
A	M1.1
ON	M1.2
=	Q1.1

NETWORK 2	
AN	I3
A	I4
=	M1.3
A	I1
A	I4
=	M1.4
AN	M1.3
O	M1.4
=	M4.2

		I1-I2	I1-I2	I1-I2	I1-I2
	a/a	00	01	10	11
I3-I4	00				
I3-I4	01				
I3-I4	10				
I3-I4	11				

Q1.1=;

ΠΑΡΑΔΕΙΓΜΑ

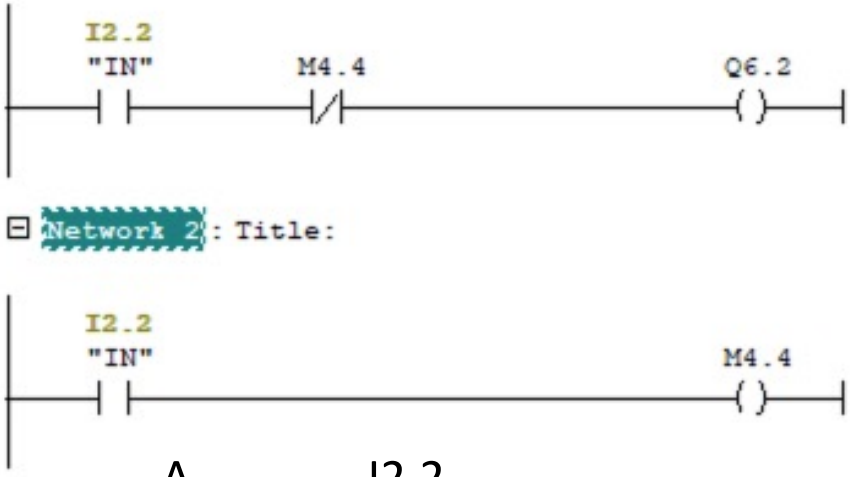
NETWORK 1	
AN	I1
A	M4.2
=	M1.1
AN	I2
A	I3
=	M1.2
AN	M1.1
O	M1.2
=	Q1.1

NETWORK 2	
AN	I3
A	I4
=	M1.3
AN	I1
A	I4
=	M1.4
A	M1.3
ON	M1.4
=	M4.2

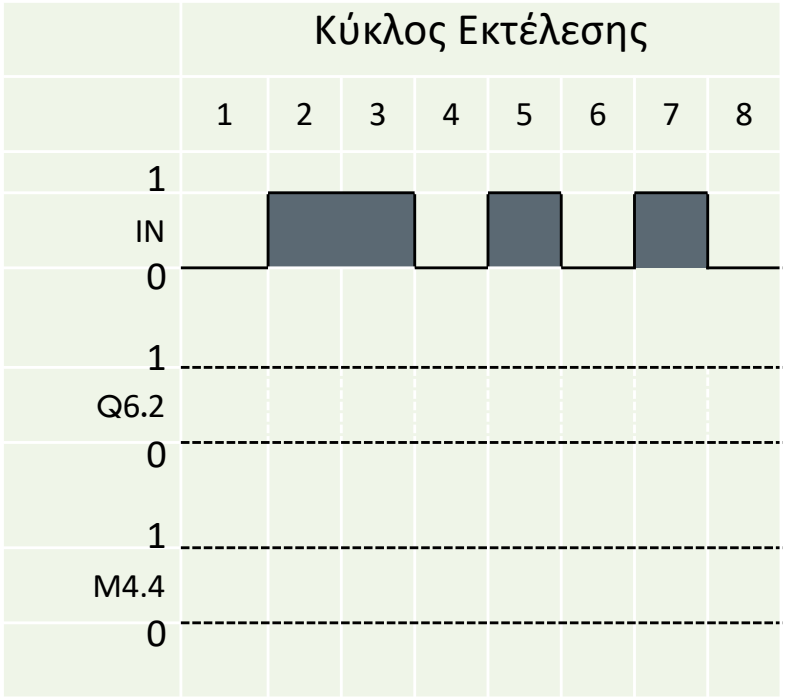
		I1-I2	I1-I2	I1-I2	I1-I2
	a/a	00	01	10	11
I3-I4	00				
I3-I4	01				
I3-I4	10				
I3-I4	11				

Q1.1=;

ΠΑΡΑΔΕΙΓΜΑ



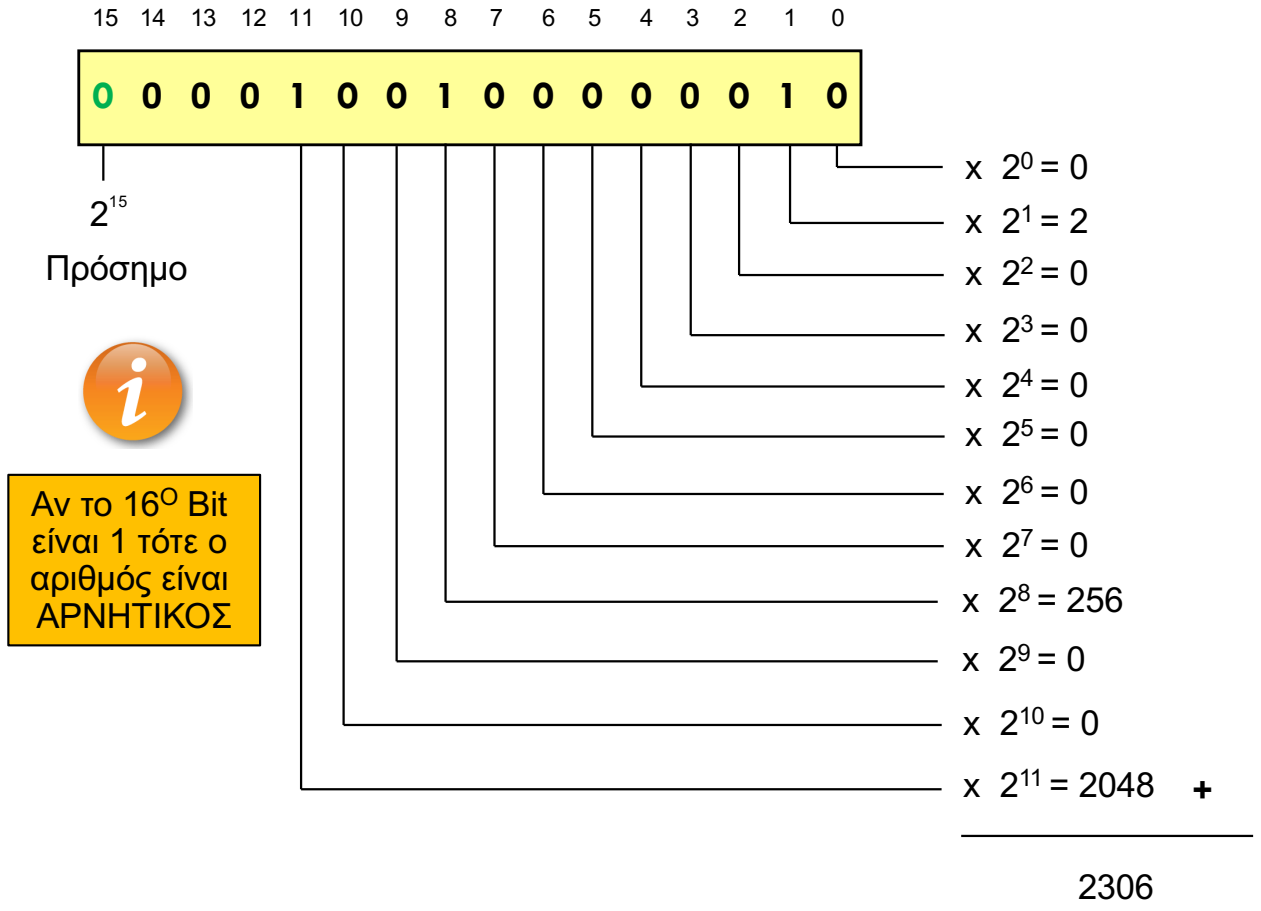

```
A     I2.2
AN    M4.4
=     Q6.2
A     I2.2
=     M4.4
```



Μεγέθη Δεδομένων

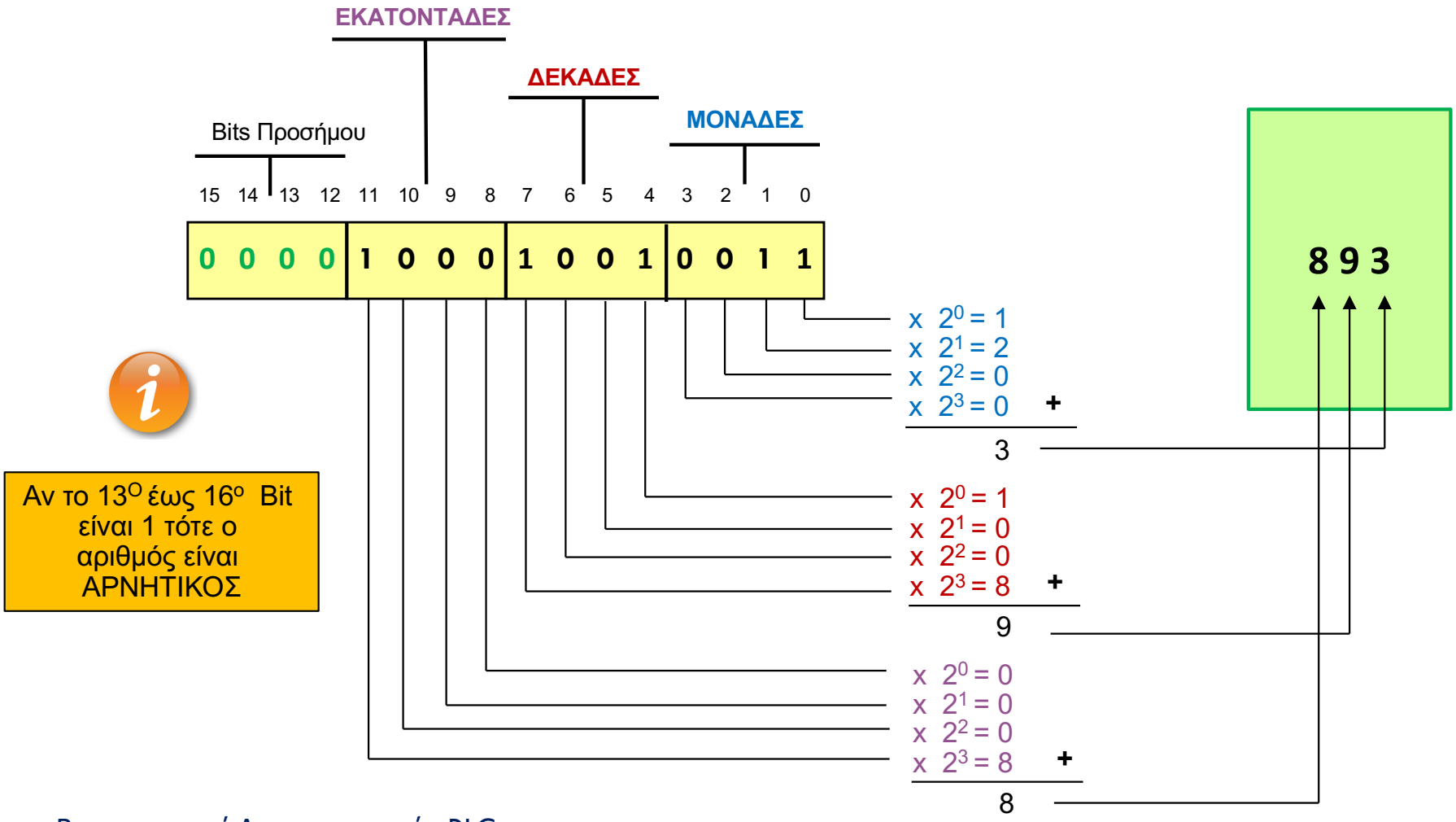
Address	BYTE							
	.7	.6	.5	.4	.3	.2	.1	.0
0	bit	bit	bit	bit	bit	bit	bit	bit
1	BYTE							
2 3	WORD							
4 5 6 7	DOUBLE WORD							
:								

INTEGER – 16Bits

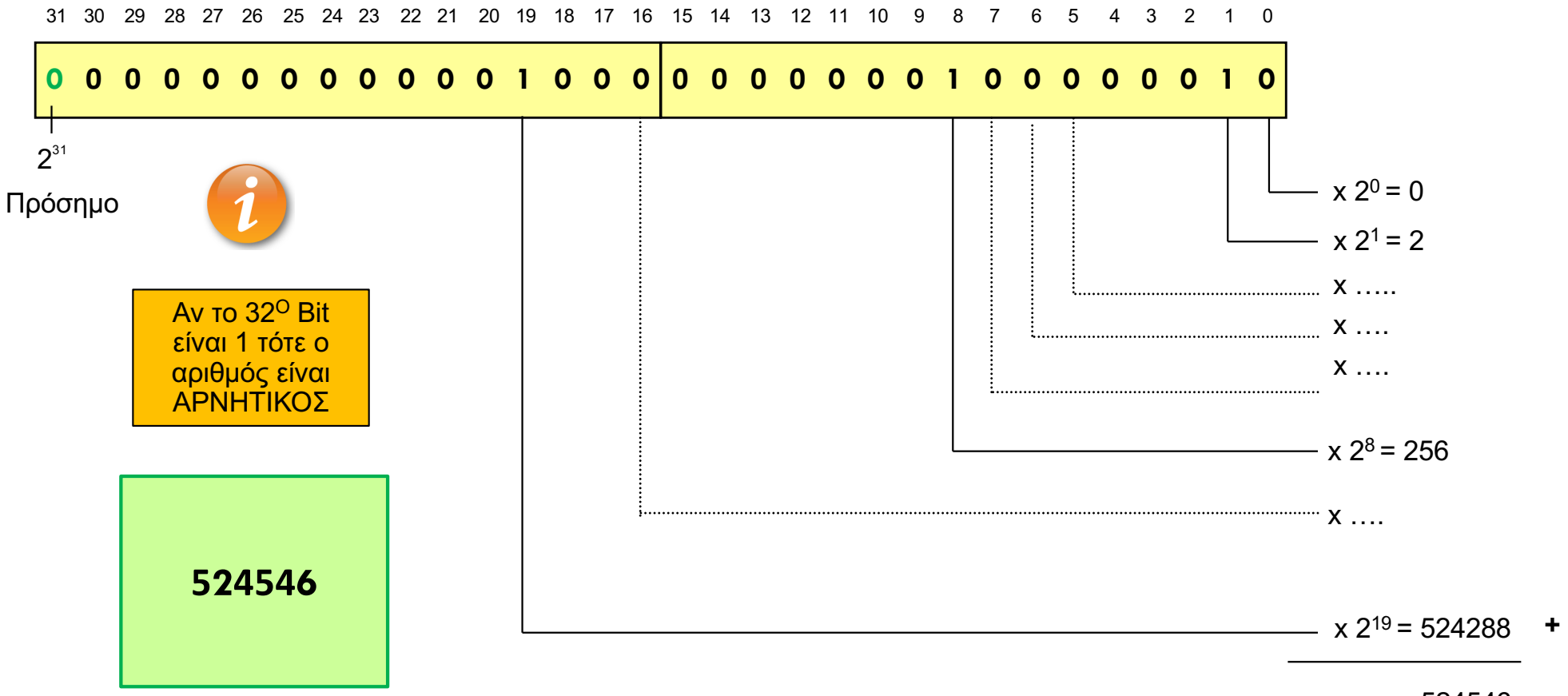


2306

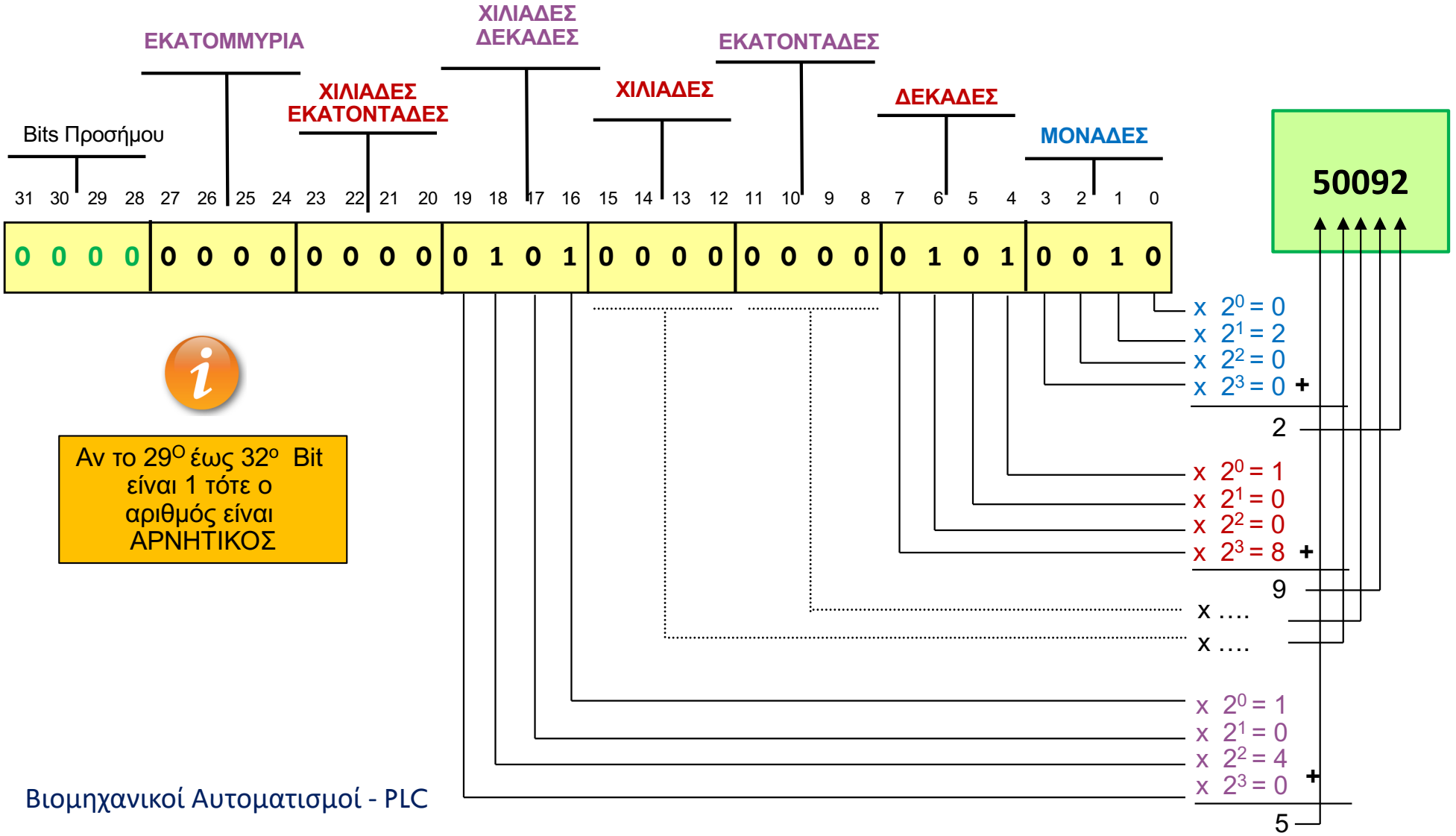
BCD – 16Bits


ΕΚΑΤΟΝΤΑΔΕΣ
ΔΕΚΑΔΕΣ
ΜΟΝΑΔΕΣ
Bits Προσήμου
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
0 0 0 0 1 0 0 0 1 0 0 1 0 0 1 1
x 2^0 = 1
x 2^1 = 2
x 2^2 = 0
x 2^3 = 0 +
3
x 2^0 = 1
x 2^1 = 0
x 2^2 = 0
x 2^3 = 8 +
9
x 2^0 = 0
x 2^1 = 0
x 2^2 = 0
x 2^3 = 8 +
8
8 9 3
Αν το 13Ο έως 16ο Bit είναι 1 τότε ο αριθμός είναι ΑΡΝΗΤΙΚΟΣ

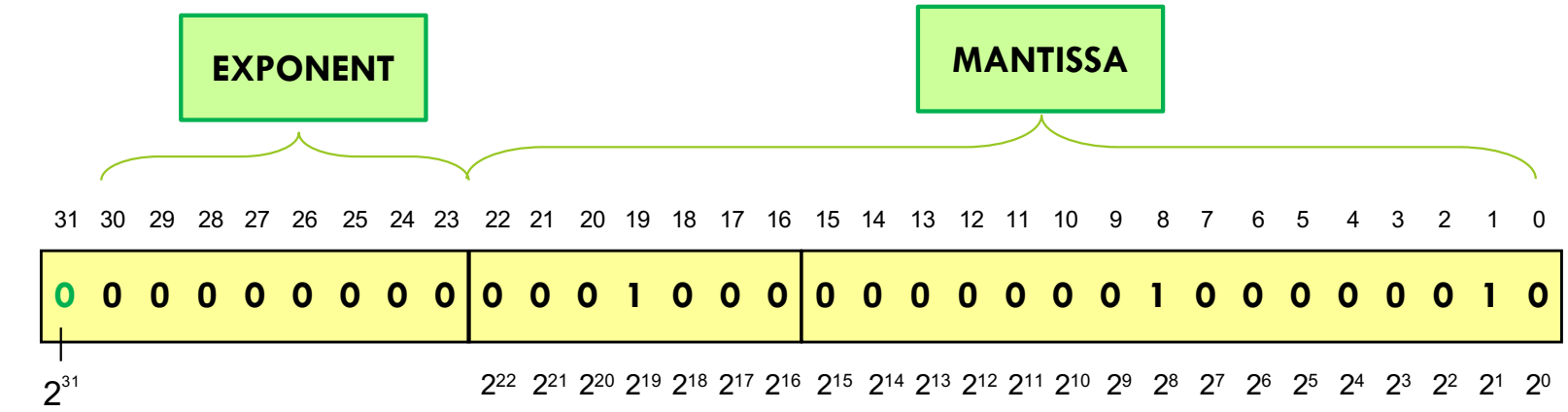
DOUBLE INTEGER – 32 Bits



DOUBLE BCD – 32 Bits

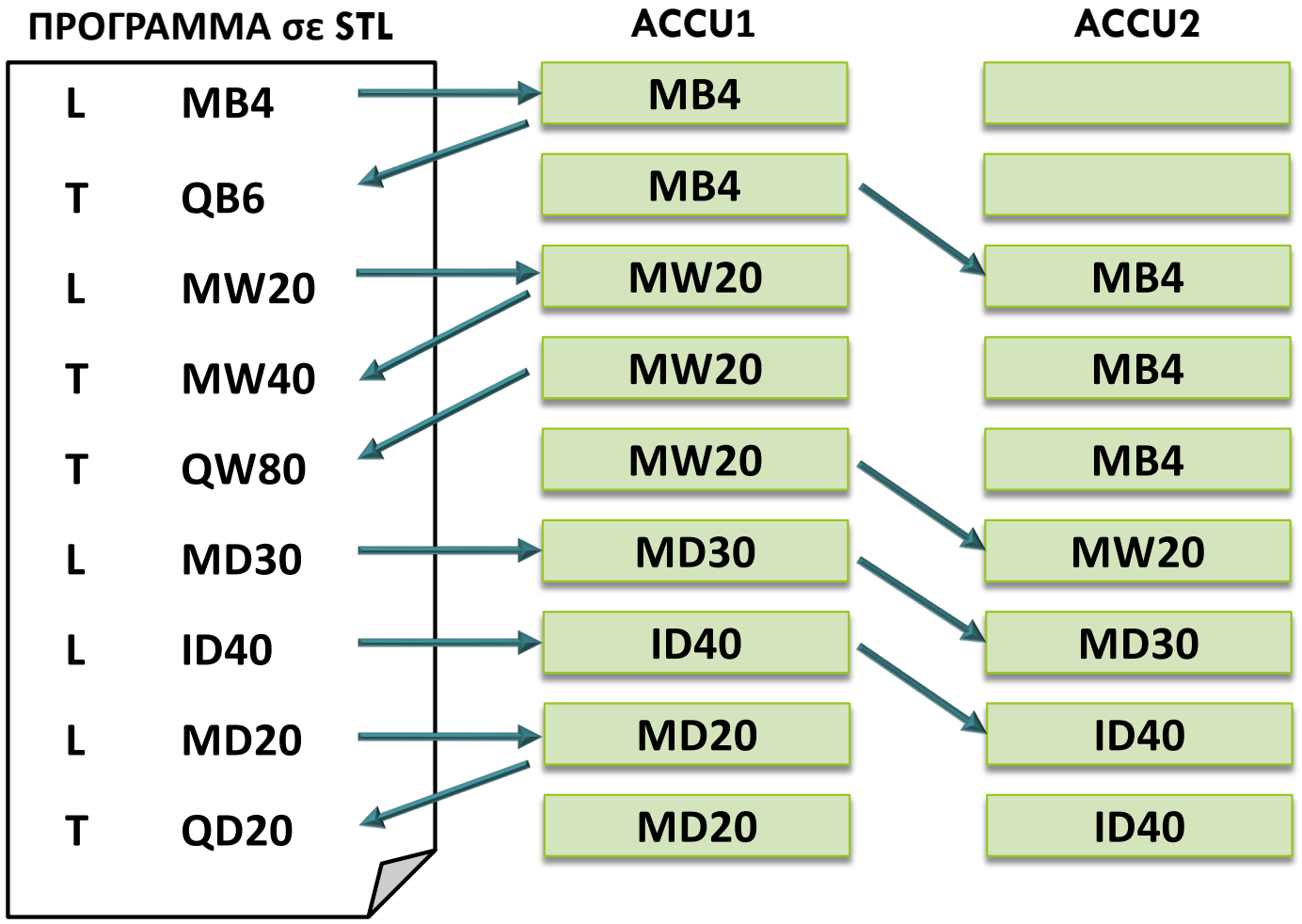


REAL

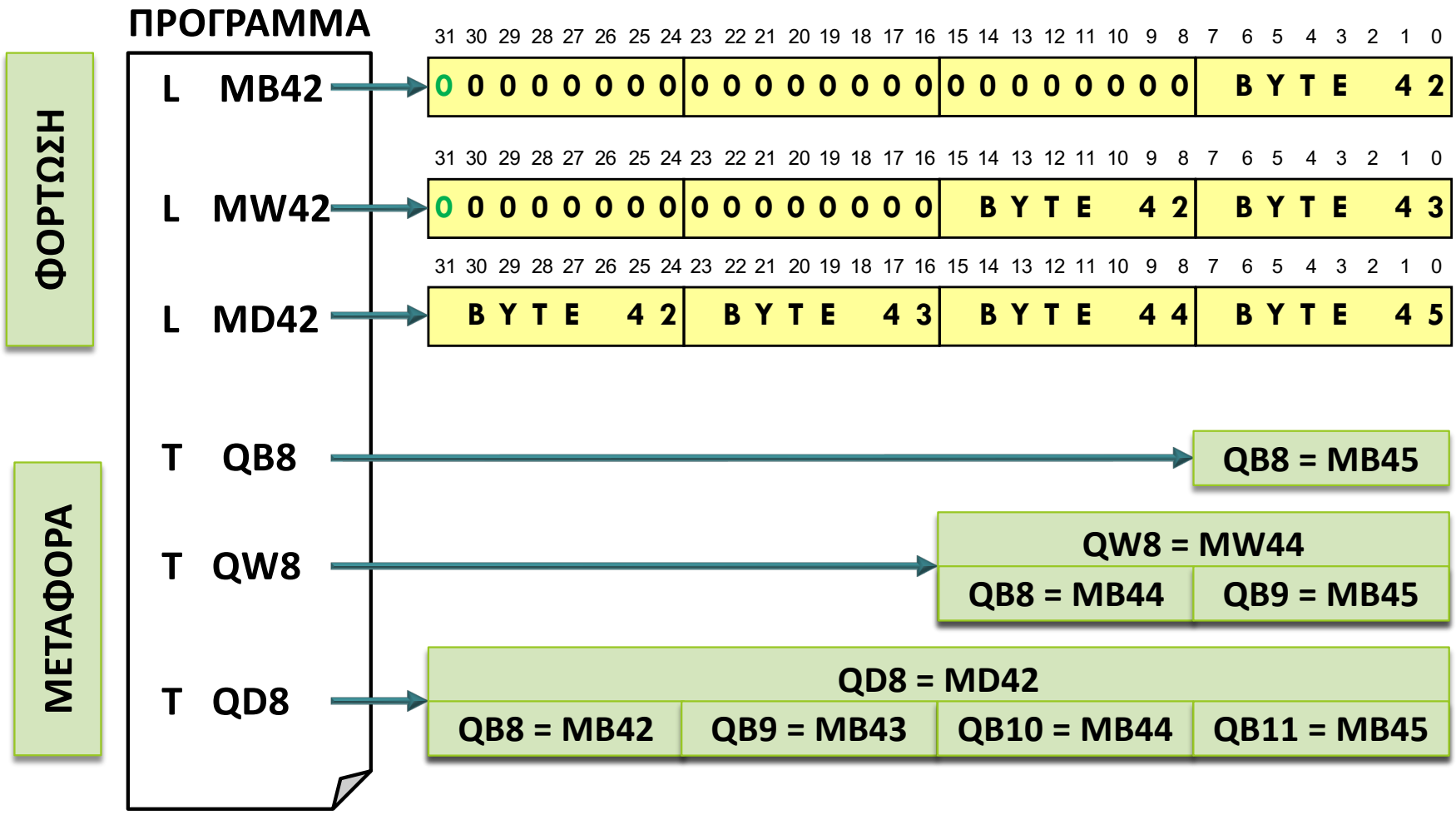


BIT πρόσημου: 2^{31} Bit
EXPONENT: 2^{30} Bit έως 2^{23} Bit
MANTISSA : 2^{22} Bit έως 2^{0} Bit

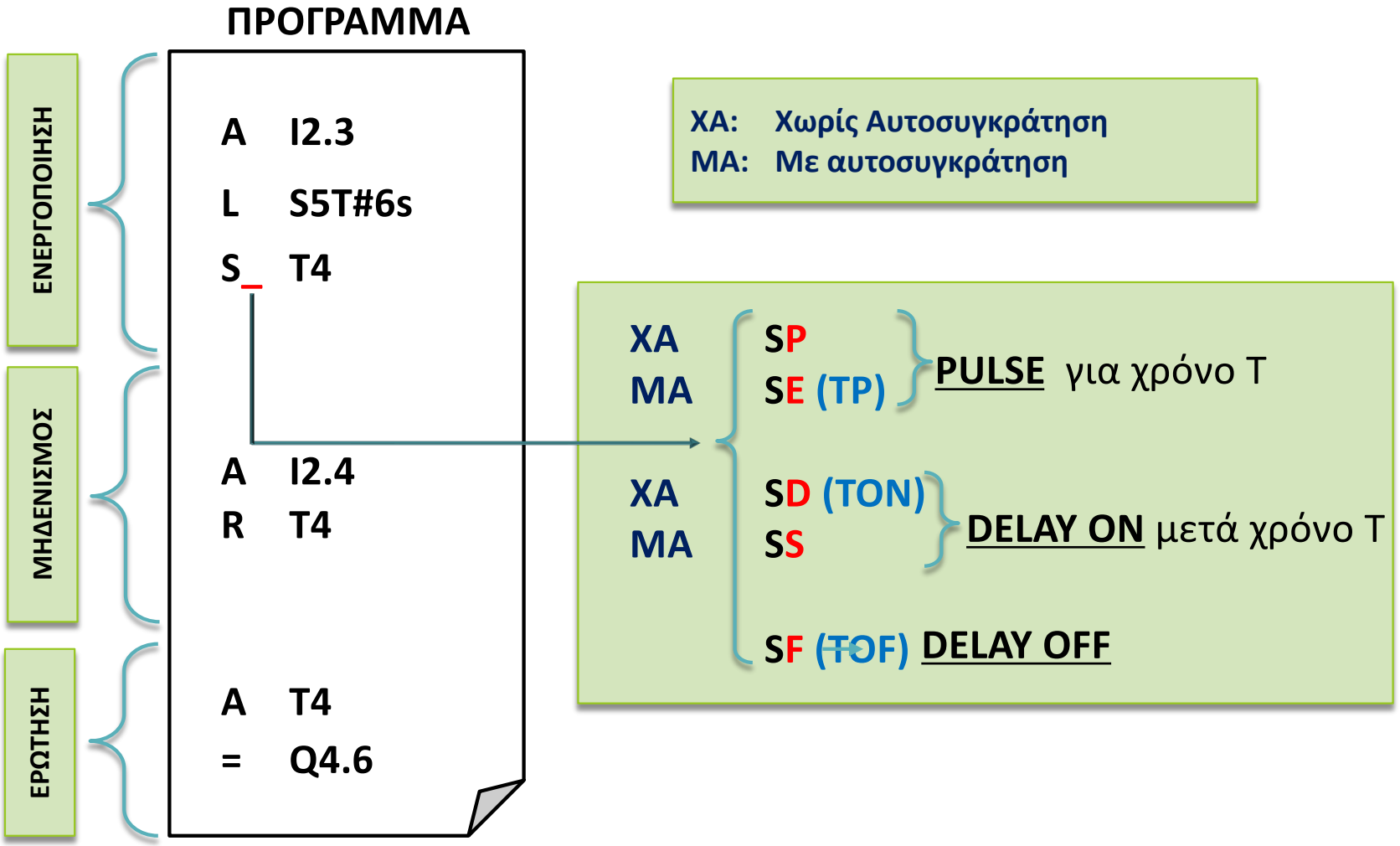
ΦΟΡΤΩΣΗ ΚΑΙ ΜΕΤΑΦΟΡΑ



ΦΟΡΤΩΣΗ ΚΑΙ ΜΕΤΑΦΟΡΑ

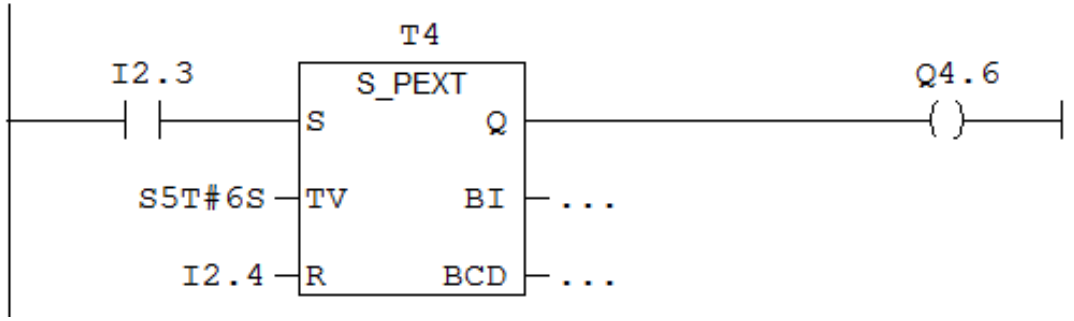


TIMERS

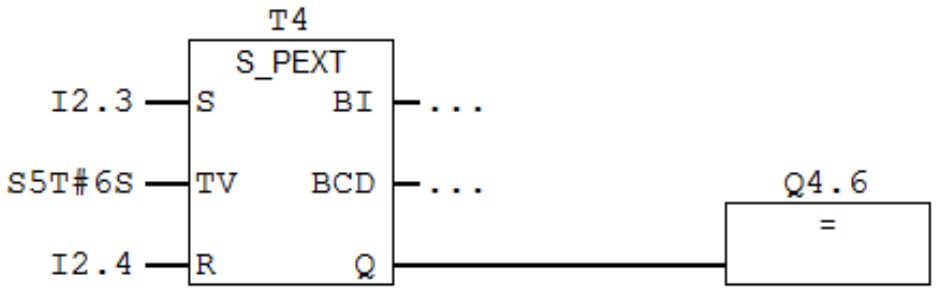

ΠΡΟΓΡΑΜΜΑ
ΕΝΕΡΓΟΠΟΙΗΣΗ
ΜΗΔΕΝΙΣΜΟΣ
ΕΡΩΤΗΣΗ
A I2.3
L S5T#6s
S_ T4
A I2.4
R T4
A T4
= Q4.6
XA: Χωρίς Αυτοσυγκράτηση
MA: Με αυτοσυγκράτηση
XA
MA
SP
SE (TP)
PULSE για χρόνο T
XA
MA
SD (TON)
SS
DELAY ON μετά χρόνο T
SF (TOF) DELAY OFF

TIMERS

LAD



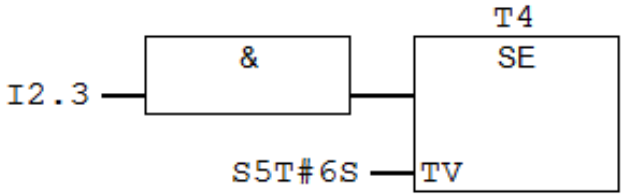
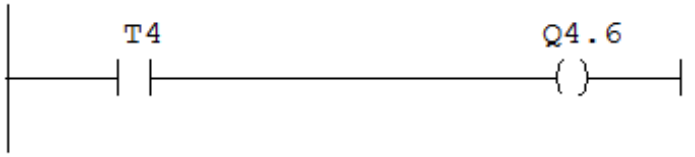
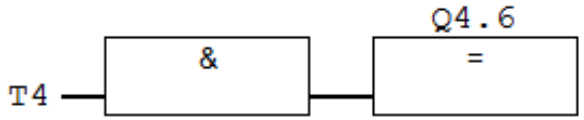
FBD



STL

```
A       I       2.3
L       S5T#6S
SE      T       4
A       I       2.4
R       T       4
NOP     0
NOP     0
A       T       4
=       Q       4.6
```

TIMERS

	LAD	FBD	STL
ΕΝΕΡΓΟΠΟΙΗΣΗ			A I 2.3 L S5T#6S SE T 4
ΜΗΔΕΝΙΣΜΟΣ			A I 2.4 R T 4
ΕΡΩΤΗΣΗ			A T 4 = Q 4.6